
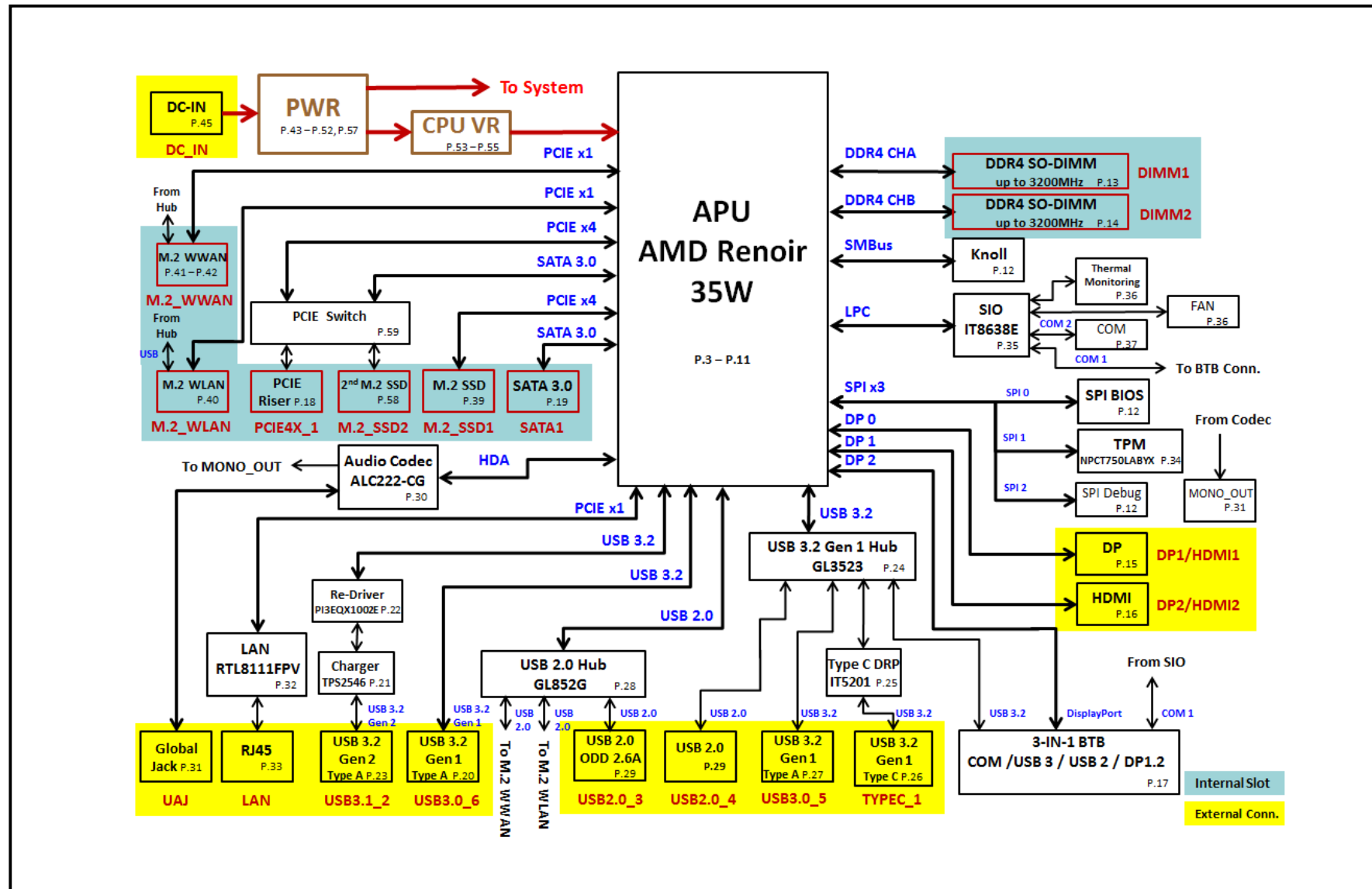


SHEET# DESCRIPTION

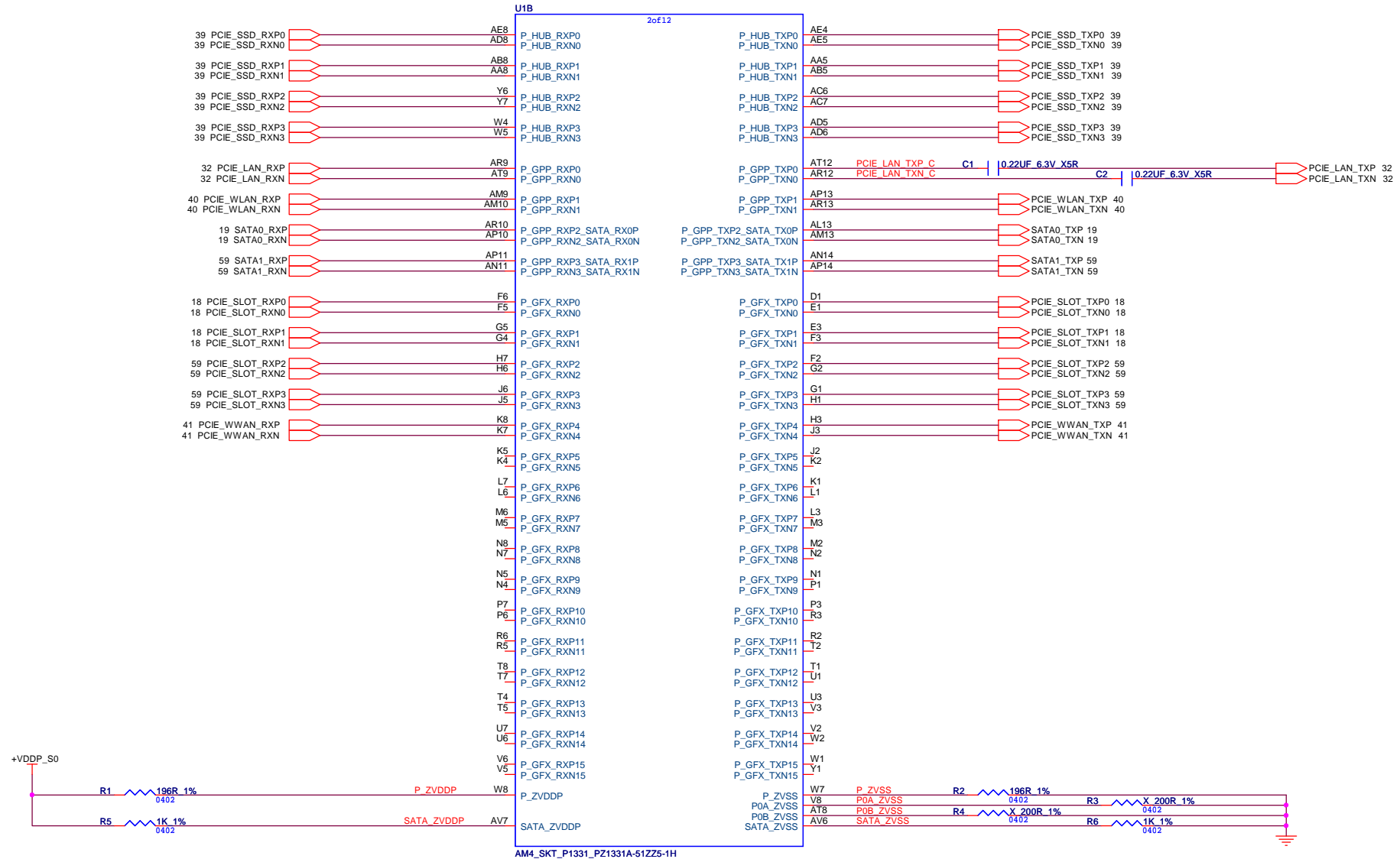
PAGE1	INDEX	PAGE31	AUDIO JACK	PAGE61	PWR DELIVERY DIAGRAM
PAGE2	BLOCK DIAGRAM	PAGE32	LAN RTL8111EPV	PAGE62	GPIO TABLE
PAGE3	AM4 PCIE I/F	PAGE33	RJ45 CONNECTOR	PAGE63	SMB MAP
PAGE4	AM4 MEM DDR4 CHA	PAGE34	TPM	PAGE64	CLOCK DIAGRAM
PAGE5	AM4 MEM DDR4 CHB	PAGE35	SIO IT8638E_BX	PAGE65	BLANK
PAGE6	AM4 DISPLAY/MISC	PAGE36	CPU FAN & THERMAL	PAGE66	BLANK
PAGE7	AM4 ACPI/AZ/SD/I2C/GPIO/FCH	PAGE37	COM PORT		
PAGE8	AM4 CLK/LPC/SPI/USB/STRAP	PAGE38	CONTROL PANEL & LED		
PAGE9	AM4 POWER	PAGE39	M.2 2280-M SSD		
PAGE10	AM4 DECOUPLING	PAGE40	M.2 2230-E WLAN		
PAGE11	AM4 GND	PAGE41	M.2 3042-B WWAN 5G		
PAGE12	KNOLL & SPI ROM	PAGE42	UIM & ANT PWR CONN		
PAGE13	DDR4 SO-DIMM CHA	PAGE43	POWER SEQUENCE		
PAGE14	DDR4 SO-DIMM CHB	PAGE44	POWER DISCHARGE		
PAGE15	DP PORT	PAGE45	DC IN 20V		
PAGE16	HDMI PORT	PAGE46	+VDDP_S5		
PAGE17	BTB CONNECTOR	PAGE47	+3V3_DSW_5V_S5		
PAGE18	PCIEX4	PAGE48	VCC3V/5V SW		
PAGE19	SATA FFC	PAGE49	+1V8_S5/+1V8_S0		
PAGE20	REAR USB 3.2 GEN1 (TIO)	PAGE50	+2V5_VPP_DDR_S3		
PAGE21	USB CHARGING	PAGE51	+1V2_MEM_S3		
PAGE22	USB3.1 GEN2 REDRIVER	PAGE52	+12V/+1V5+S5		
PAGE23	FRONT USB 3.2 GEN2	PAGE53	VDDCR PWM IC		
PAGE24	USB 3.0 HUB	PAGE54	VDDCR_CPU		
PAGE25	TYPE C PWR & MUX	PAGE55	VDDCR_SOC		
PAGE26	FRONT USB TYPE C PORT	PAGE56	SCREW HOLE		
PAGE27	REAR USB 3.2 GEN1 (UPO)	PAGE57	GFX 12V		
PAGE28	USB 2.0 HUB	PAGE58	M.2 2242 SSD		
PAGE29	REAR USB 2.0 (ODD & STD)	PAGE59	PCIE SWITCH & CLK BUFFER		
PAGE30	AUDIO CODEC ALC222	PAGE60	PWR SEQUENCE DIAGRAM		

 Universal Scientific Industrial Co., Ltd.		
TITLE: TINY6 M75Q-2 INDEX		REV: V0.3
Document Number : <Doc>		
Prepared by : Jason		
SIZE : A3	Date: Tuesday, April 28, 2020	PAGE: 1 of 66

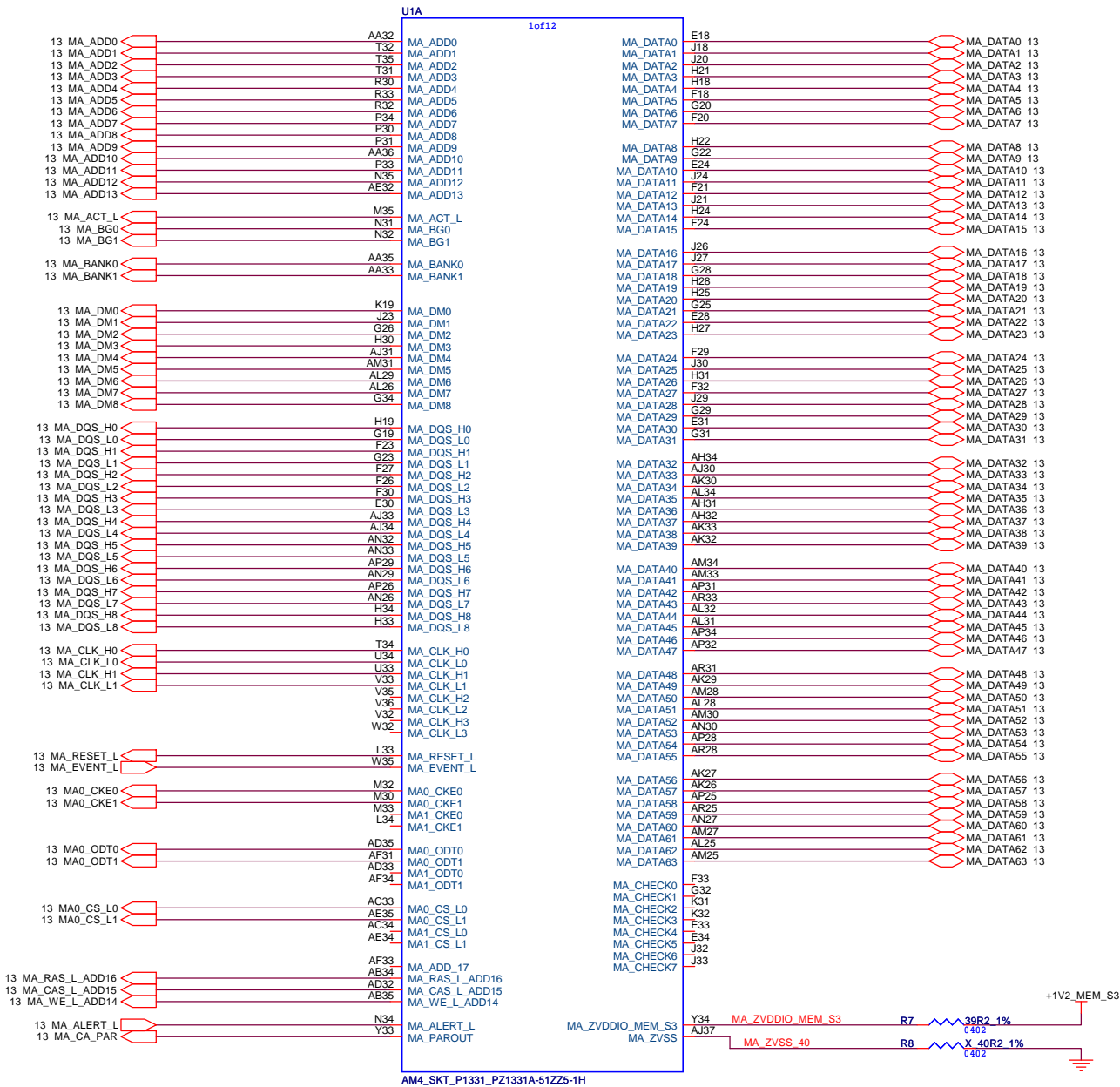
BLOCK DIAGRAM



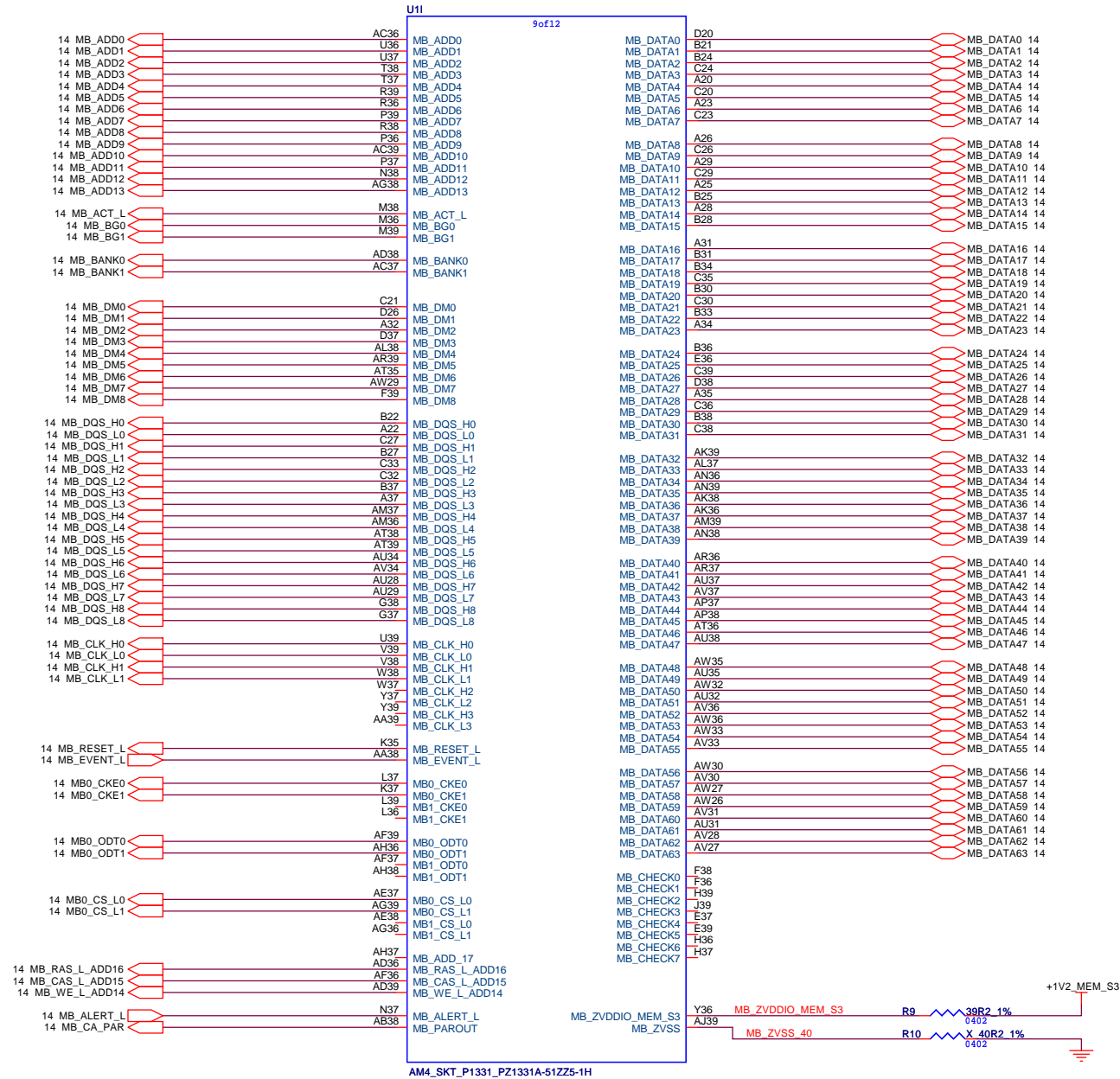
AM4 PCIE I/F



AM4 MEM DDR4 CHA

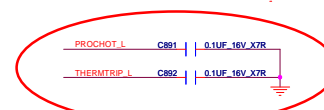
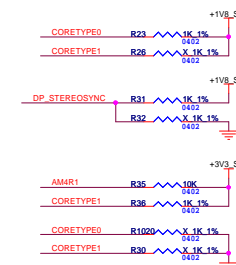
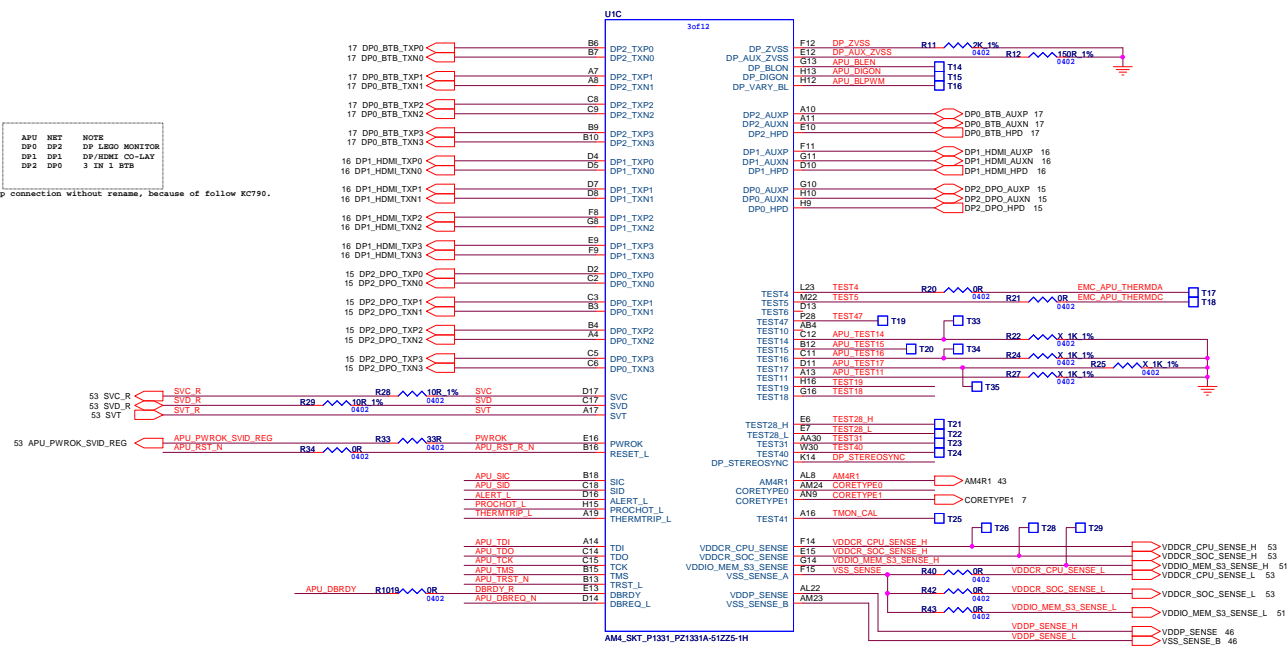


AM4 MEM DDR4 CHB

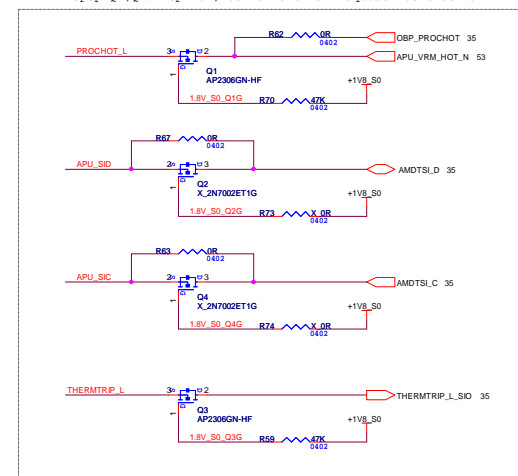
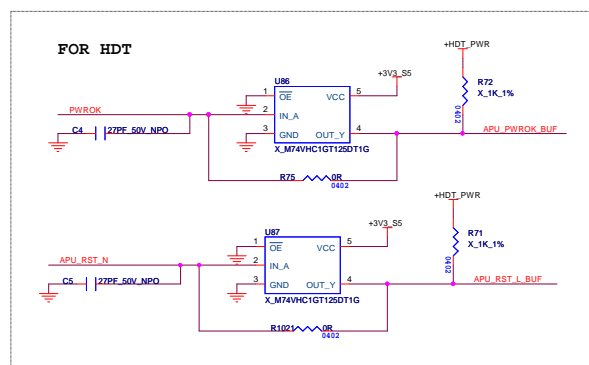
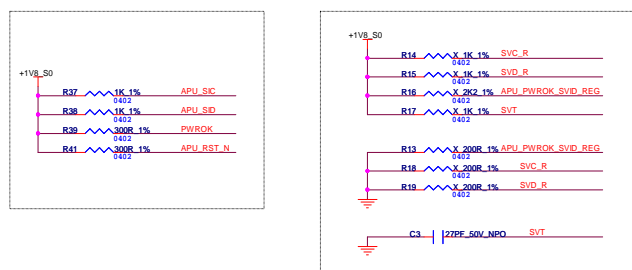


APU	NET	NOTE
DP0	DP2	DP LEGO MONITOR
DP1	DP1	DP/HDMI CO-LAY
DP2	DP0	3 IN 1 STR

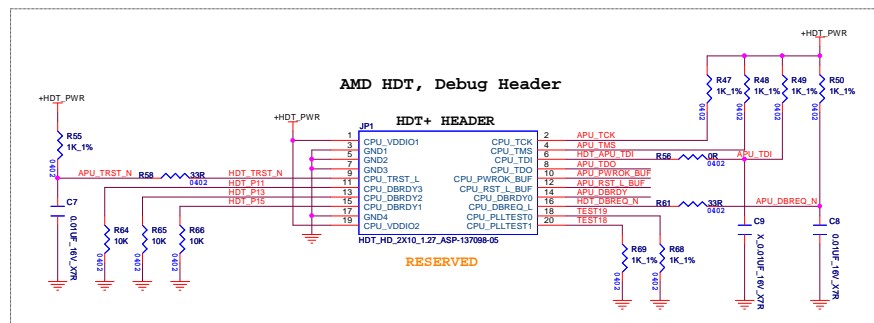
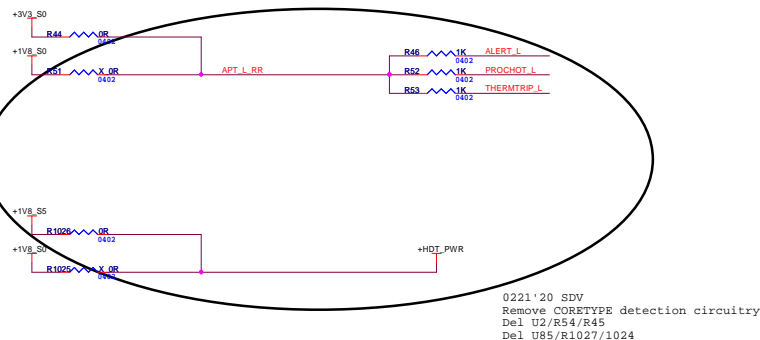
* Swap connection without rename, because of follow KC790.

0226'20 V03
Add C891, C892 for SI fine tune

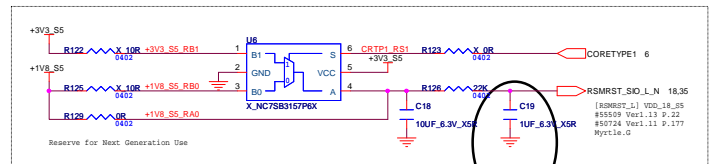
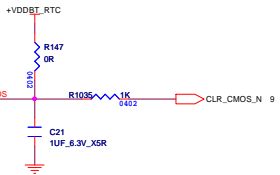
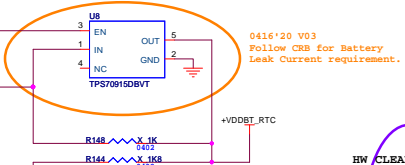
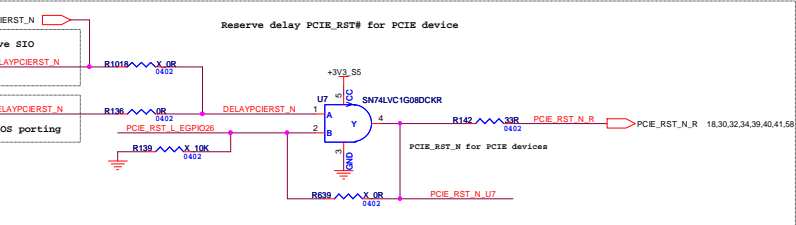
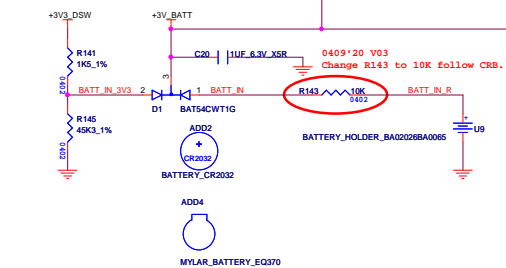
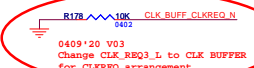
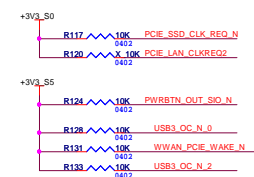
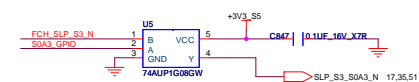
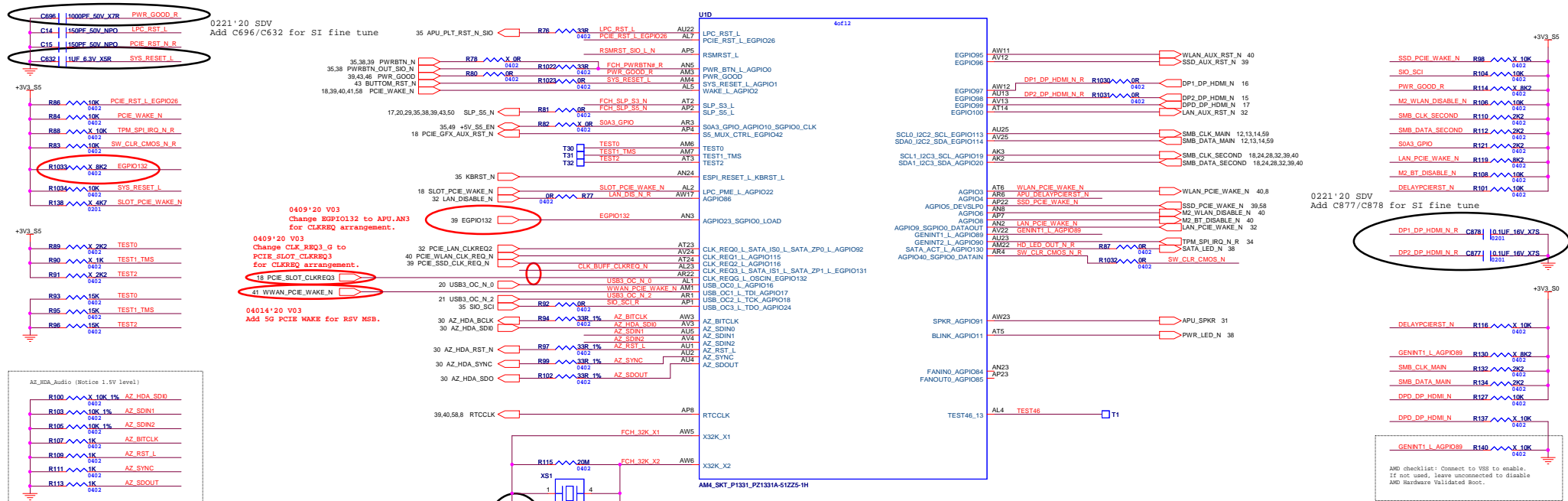
Depop Q2,Q4. Pop R67,R63 for thermal request X03 0408Y19



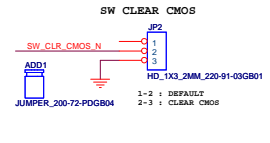
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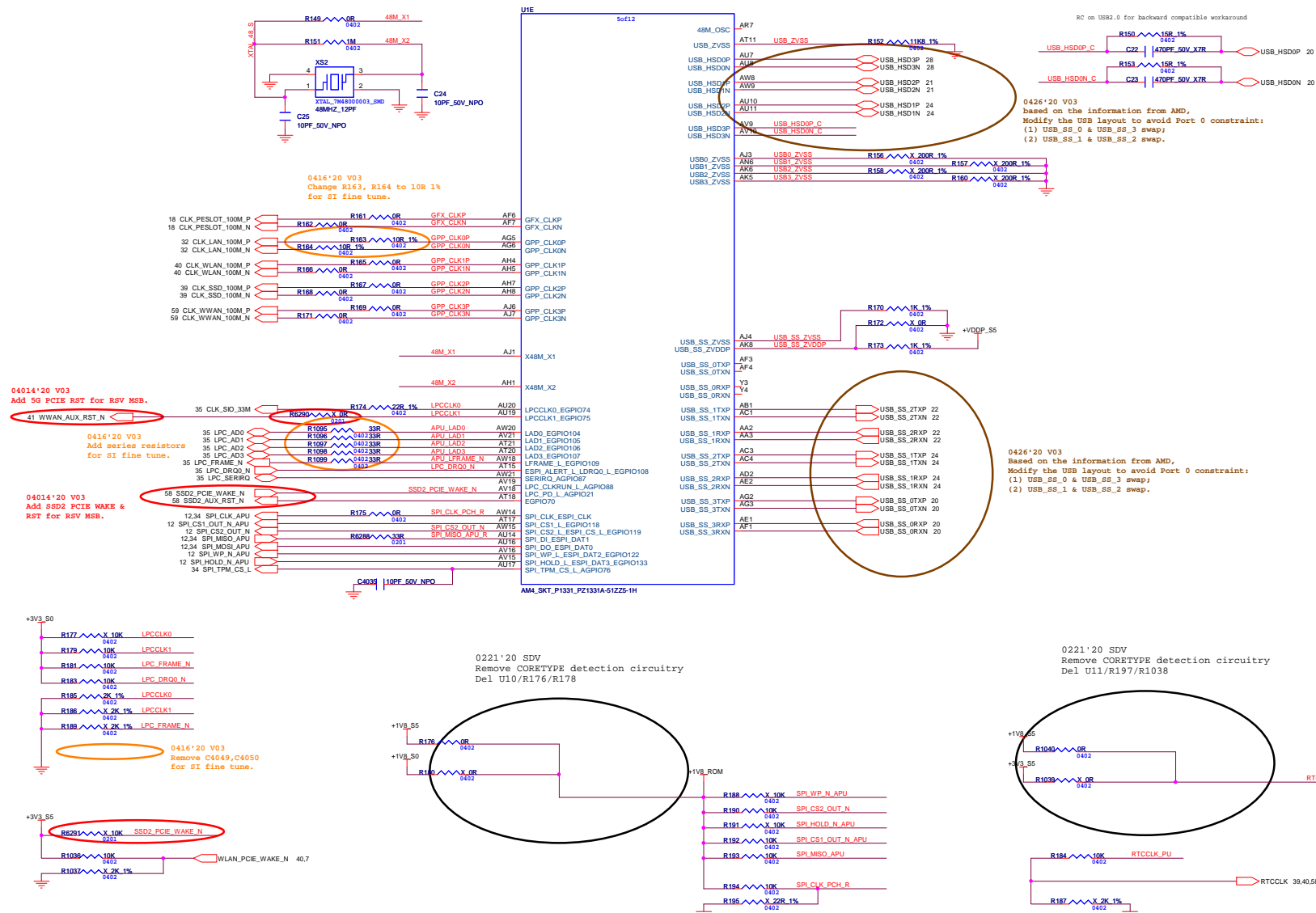


AM4 ACPI/AZ/SD/I2C/GPIO/FCH



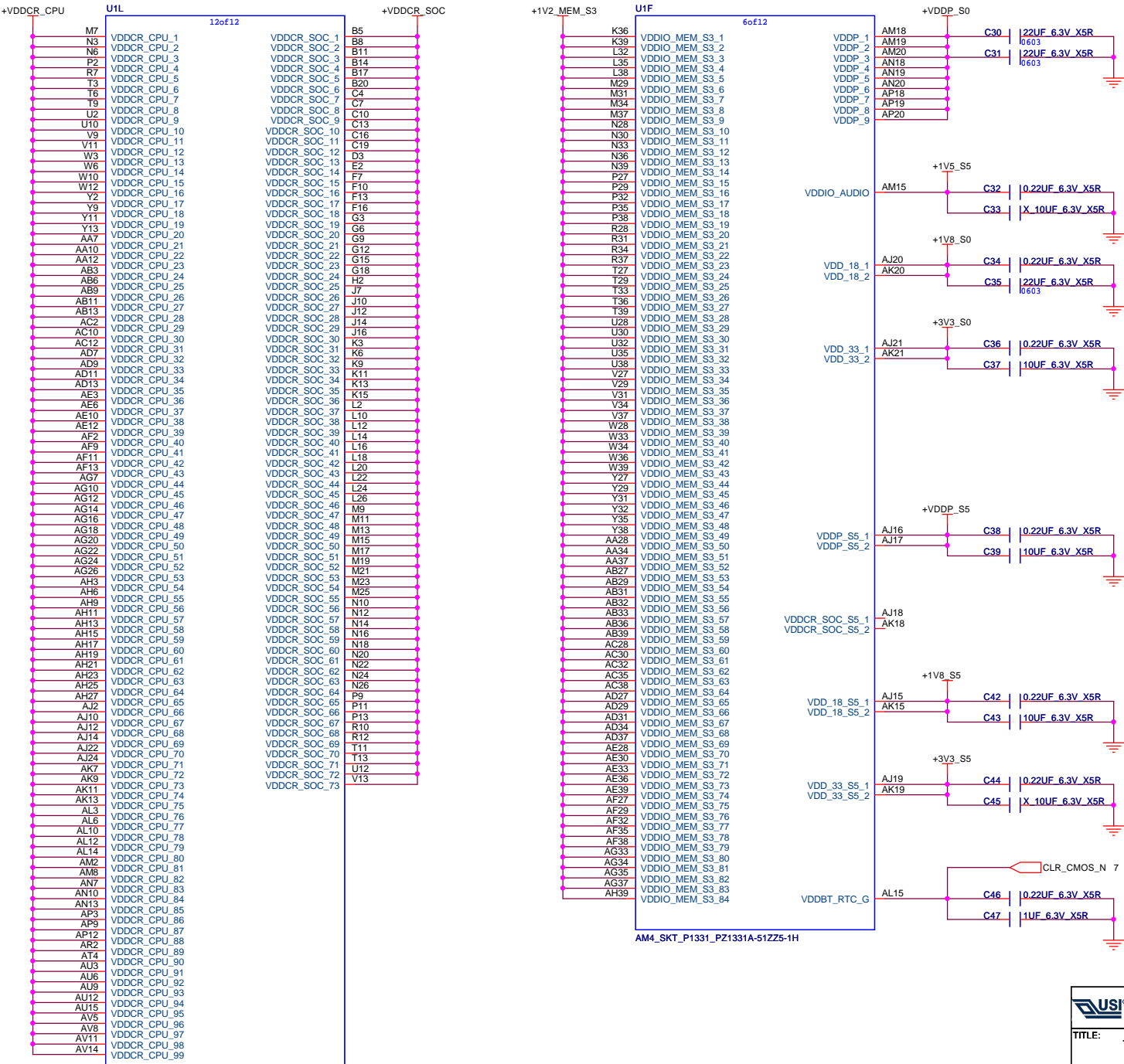
0221'20 SDV
Change C19 0.1uF --> 1uF for timing tuning





Renoir Strap Table (AM4 TYPE 5)			
	SPI CLK	LFRAME_L	SYS_RST#
PULL HIGH	Internal clock mode (DEFAULT)	SPI ROM (DEFAULT)	Normal reset mode (DEFAULT)
PULL LOW	Ext clock mode	LPC ROM	Short reset mode

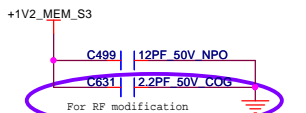
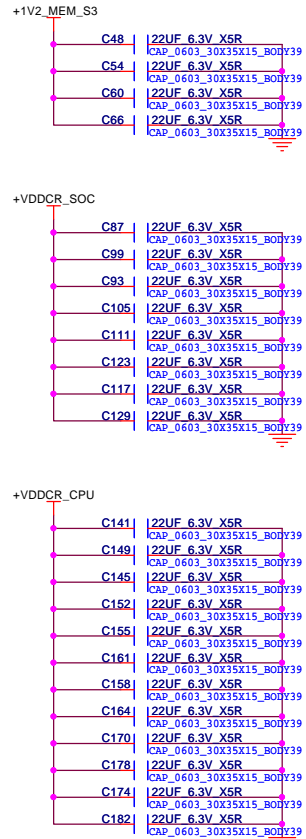
AM4 POWER



AM4_SKT_P1331_PZ1331A-51ZZ5-1H

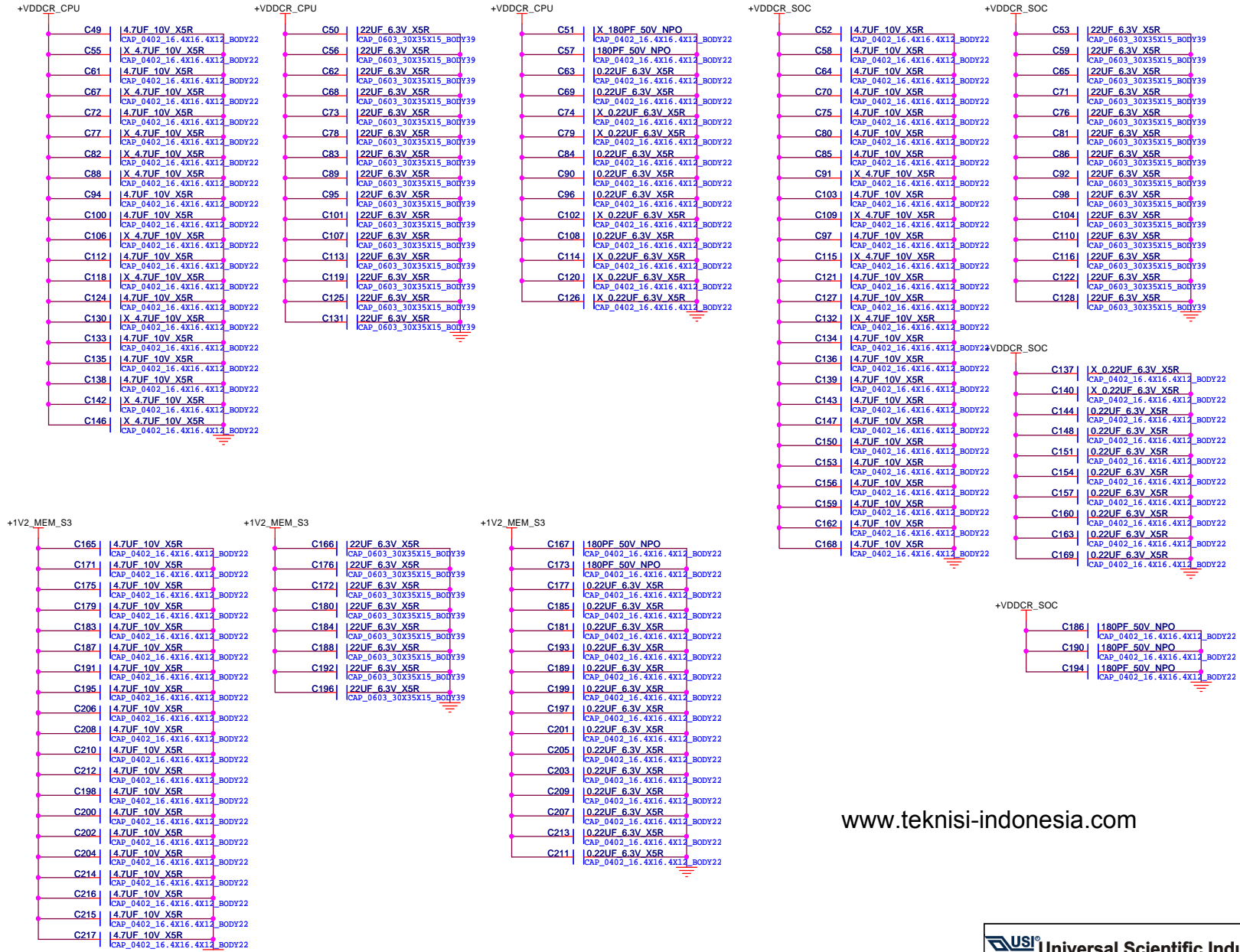
AM4 DECOUPLING

TOP CAVITY



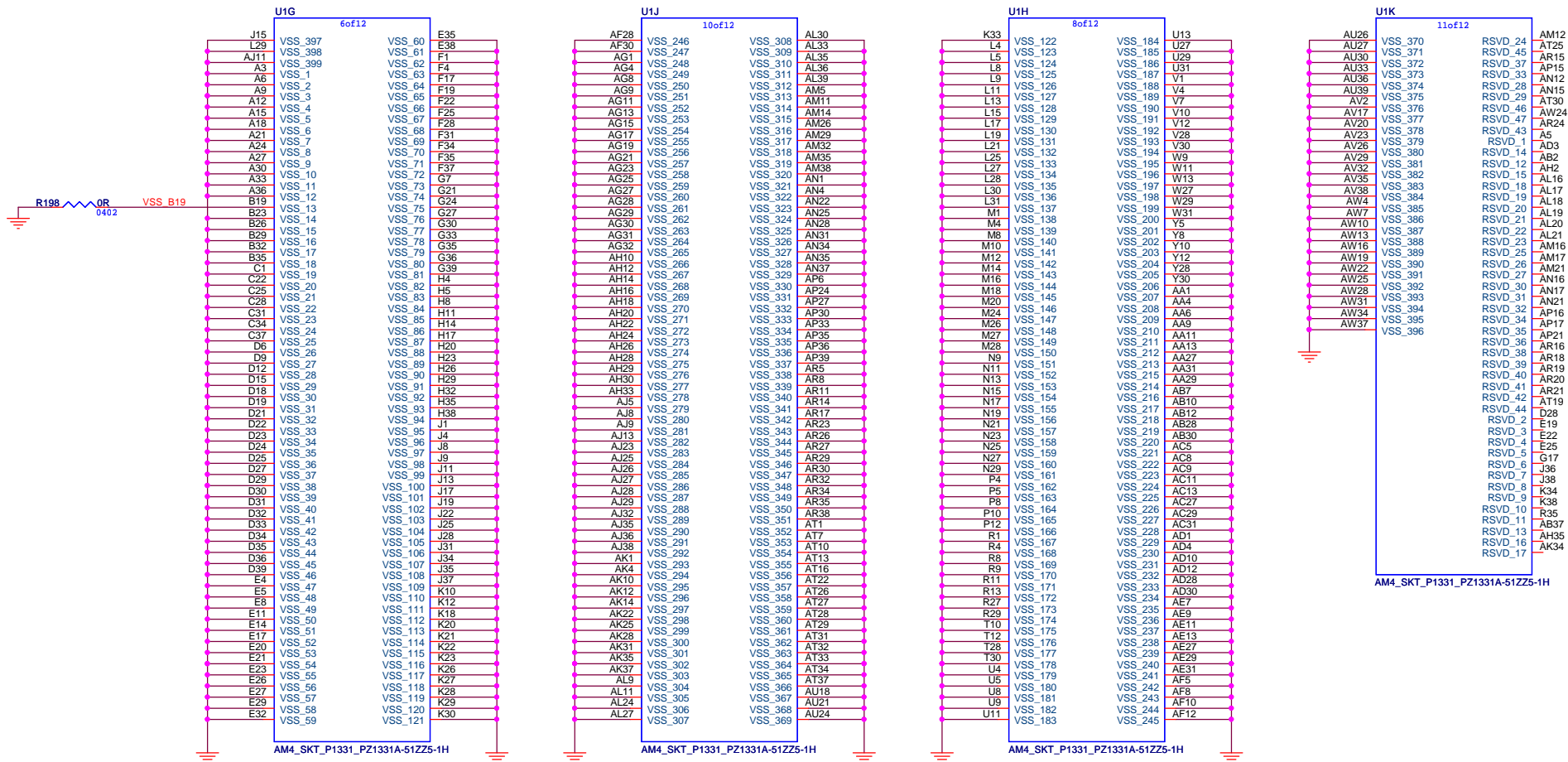
0420'20 V03
Down size by USI CM suggested.

BOTTOM SIDE DECOUPLING

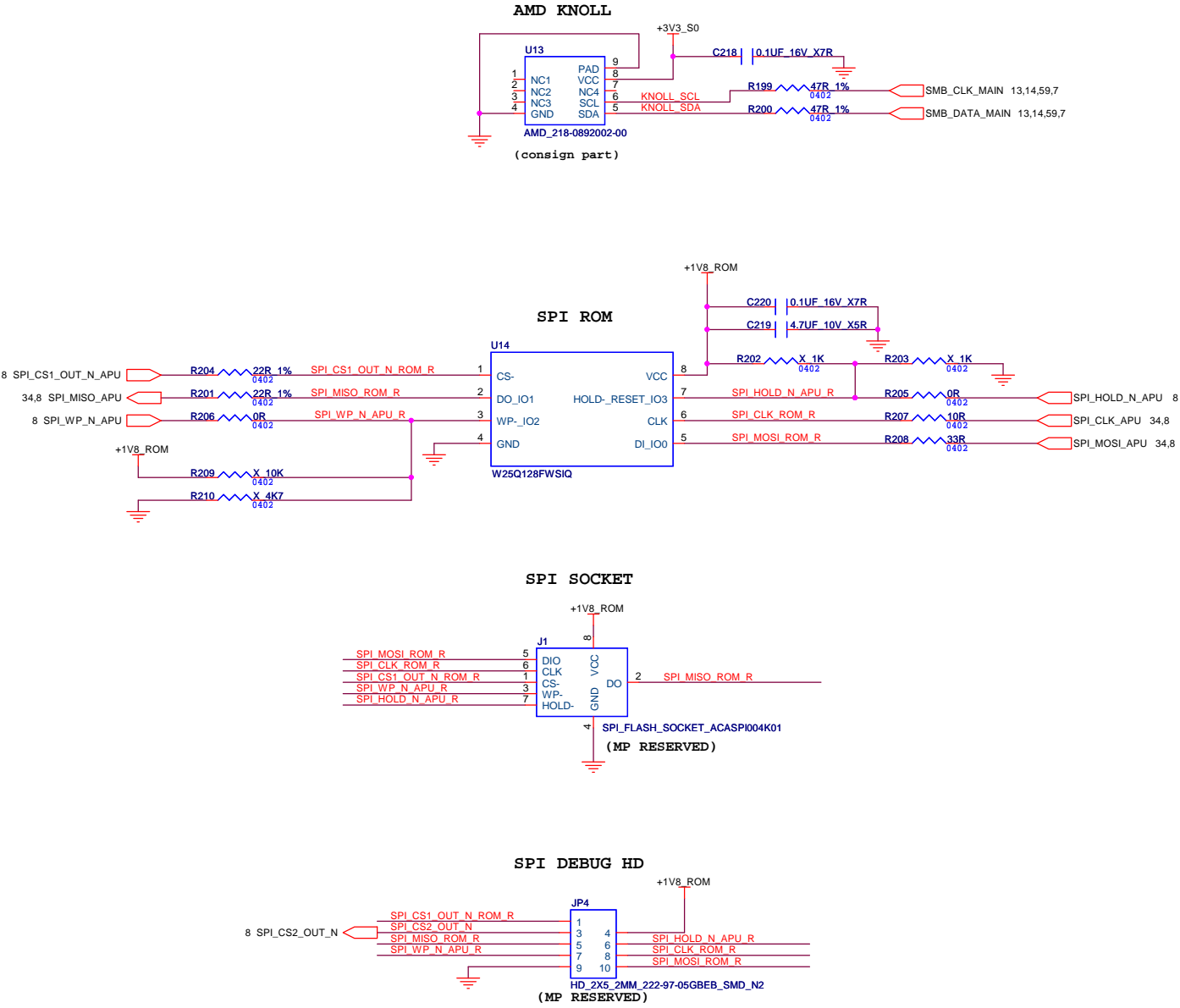


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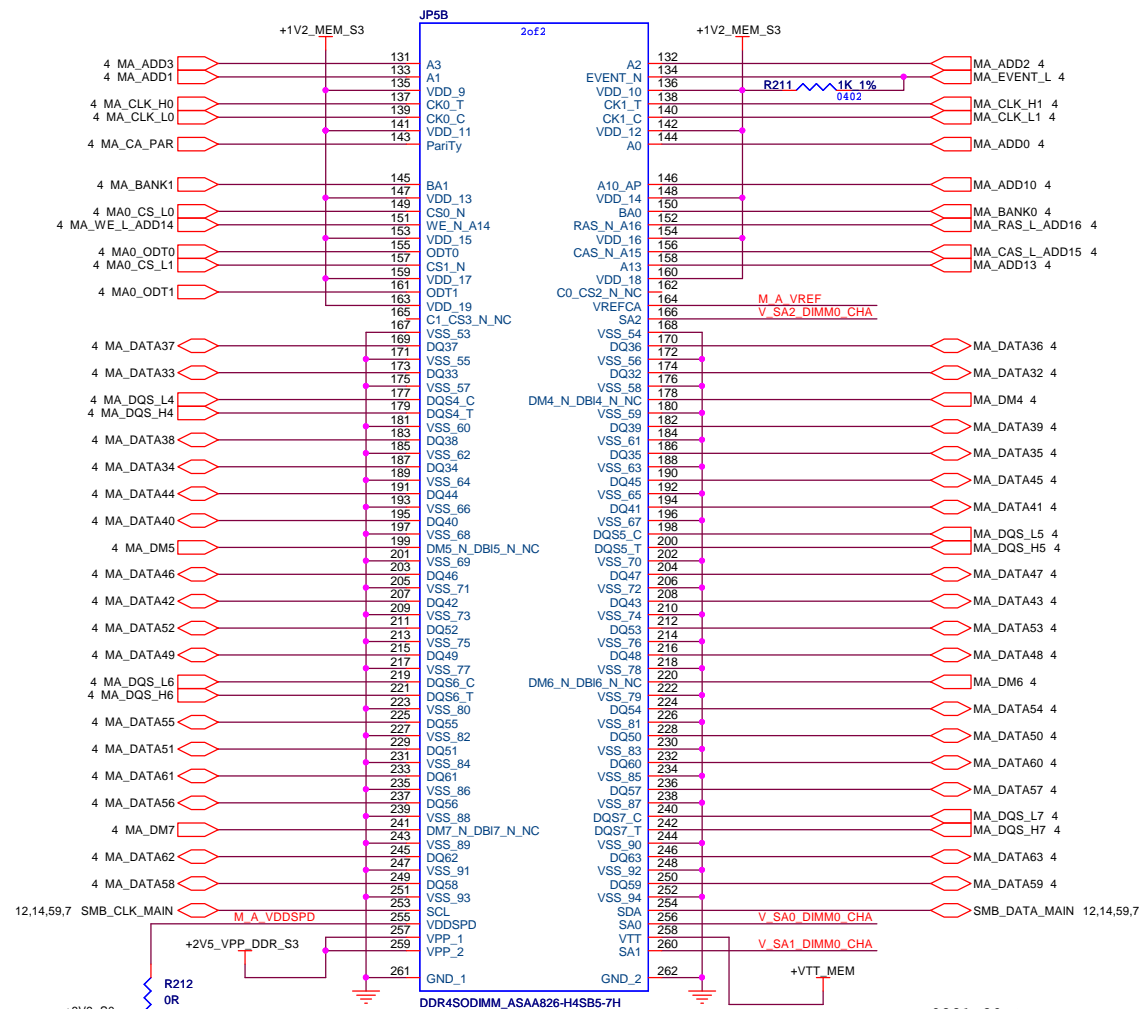
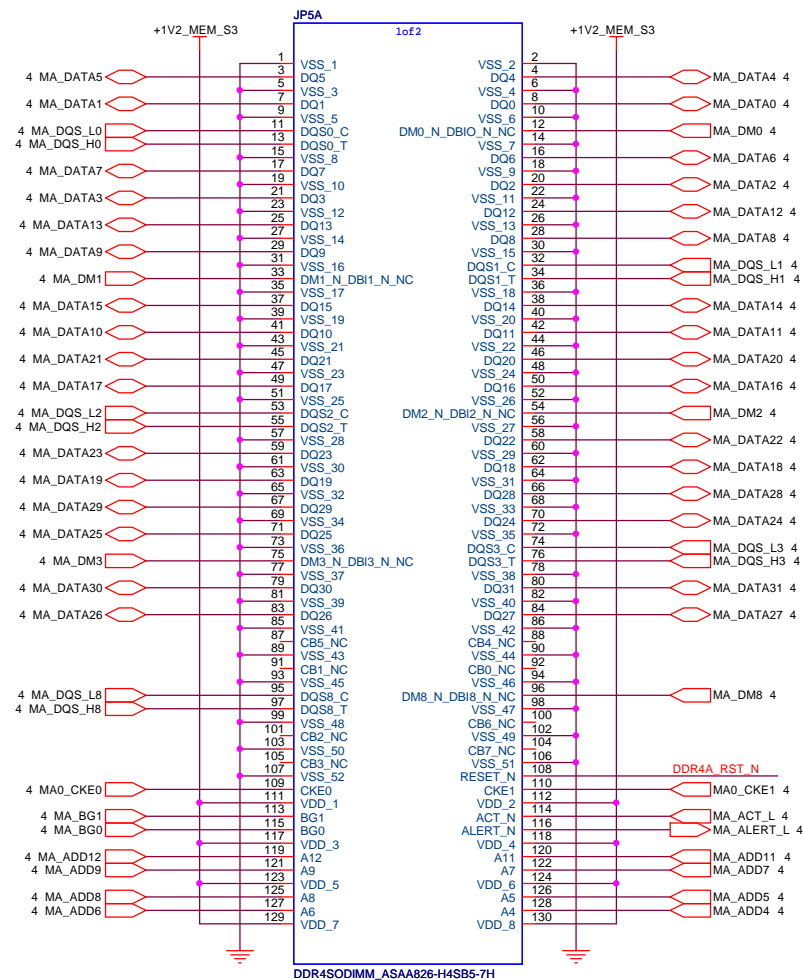
AM4 GND



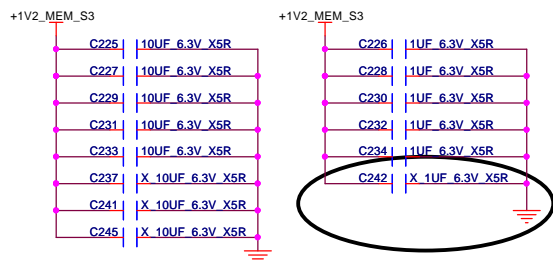
KNOLL & SPI ROM



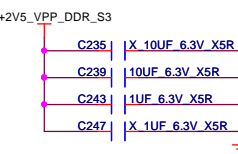
DDR4 SO-DIMM CHA



PLACE ALL CAPACITORS CLOSE TO SODIMM

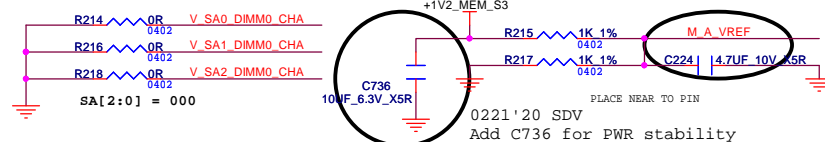


0221'20 SDV
Pop C221 180pF
for SI fine tu




PLACE ALL CAPACITORS CLOSE TO SODIMM

0420'20 V03
Down size by USI CM suggested.

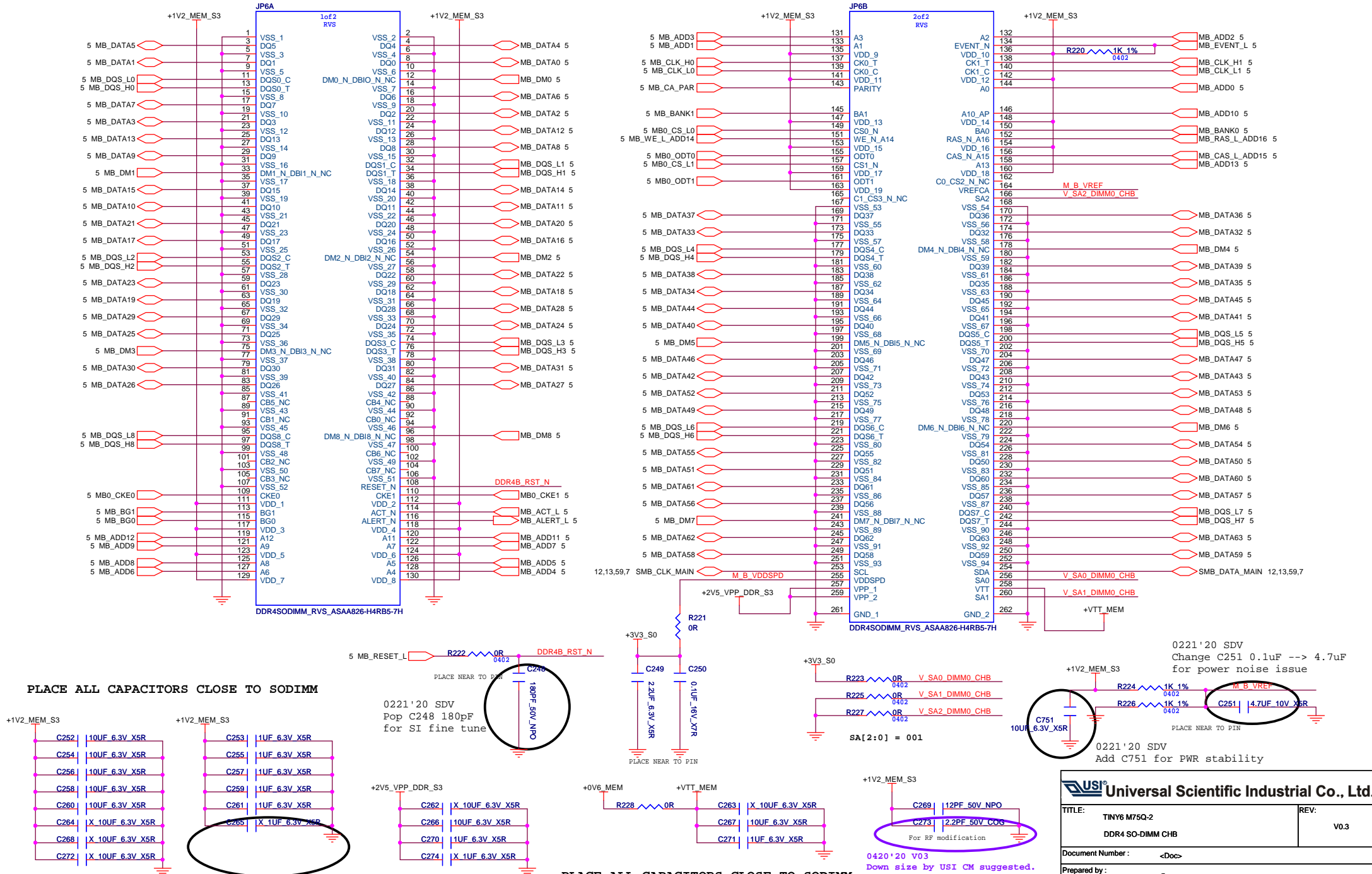


0221'20 SDV
Change C224 0.1uF --> 4.7uF
for power noise issue

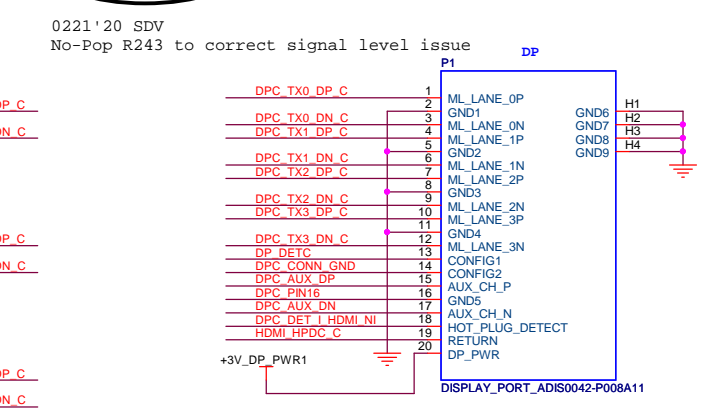
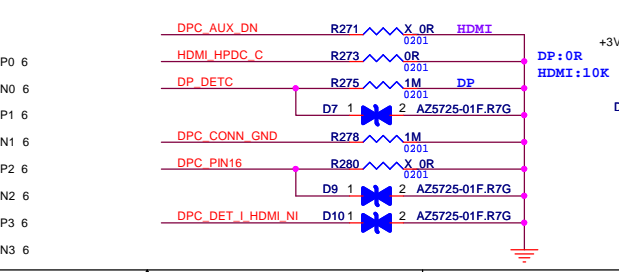
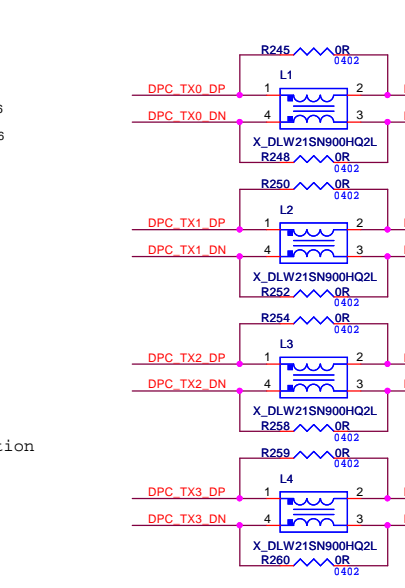
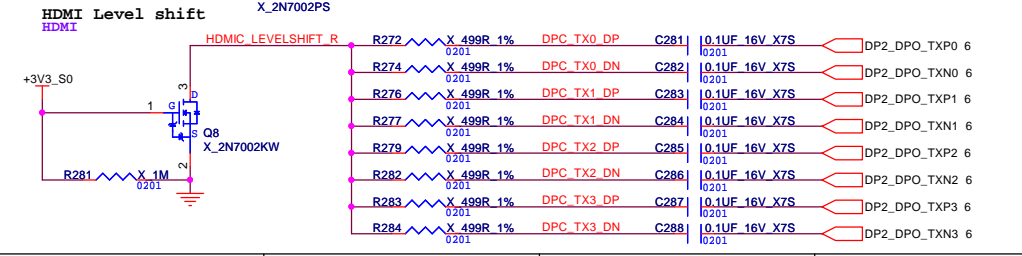
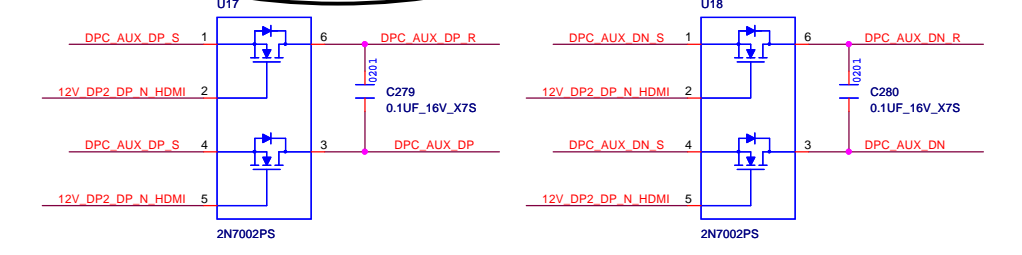
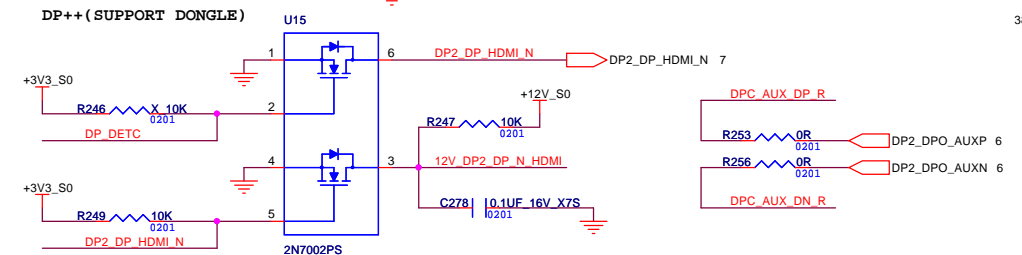
0221'20 SDV
Add C736 for PWR stability

 Universal Scientific Industrial Co., Ltd.			
TITLE: TINY6 M75Q-2 DDR4 SO-DIMM CHA		REV: V0.3	
Document Number : <Doc>			
Prepared by : <i>Tason</i>			
SIZE : A3	Date: Tuesday, April 28, 2020	PAGE: 13 of 66	

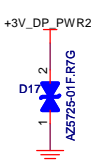
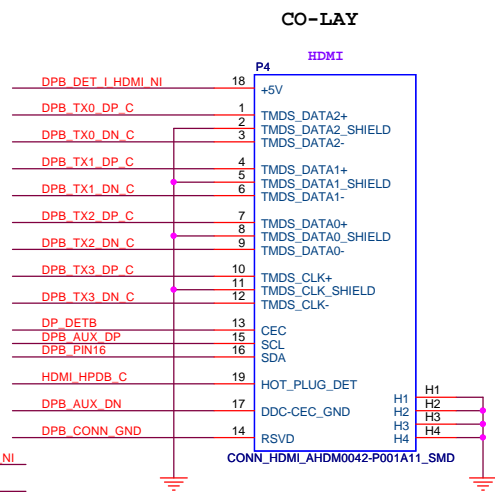
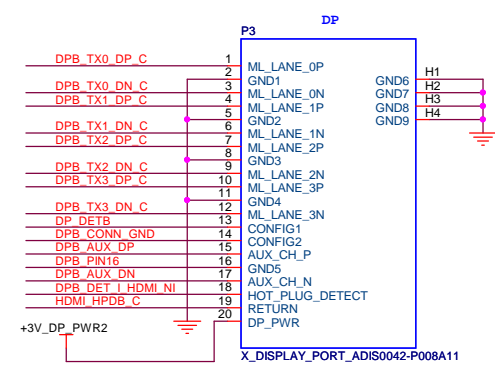
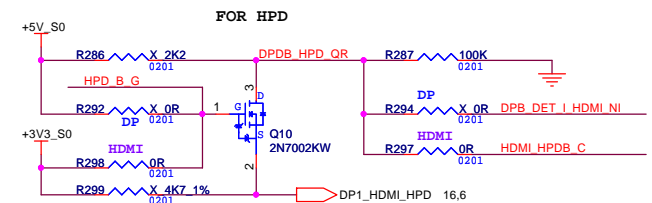
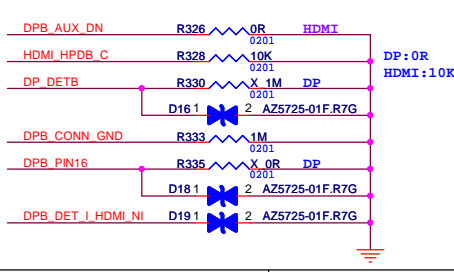
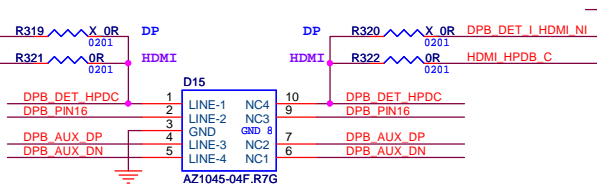
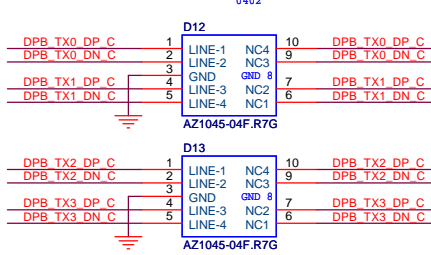
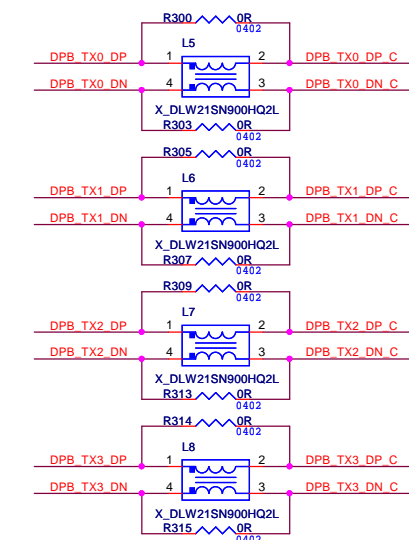
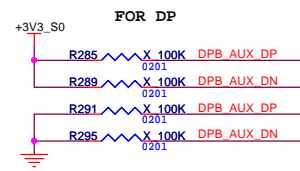
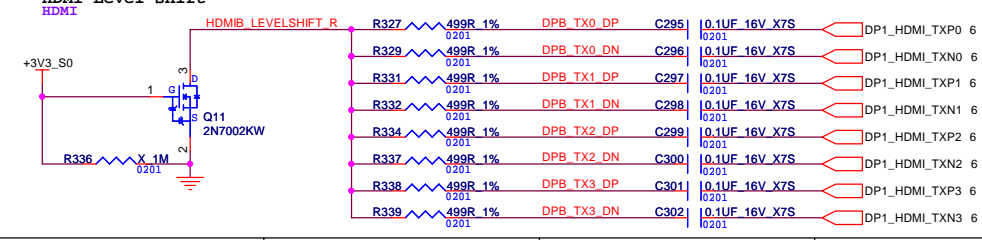
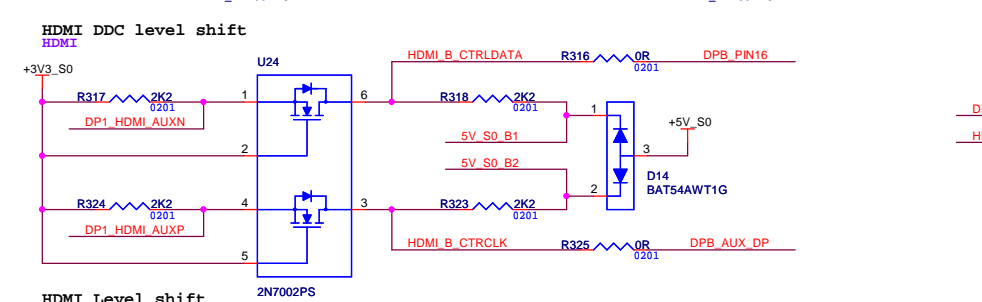
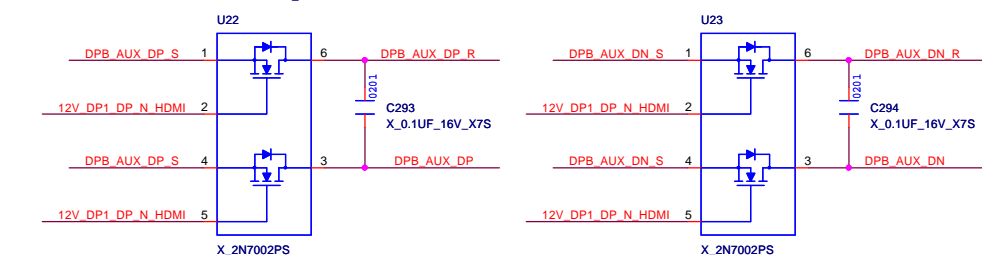
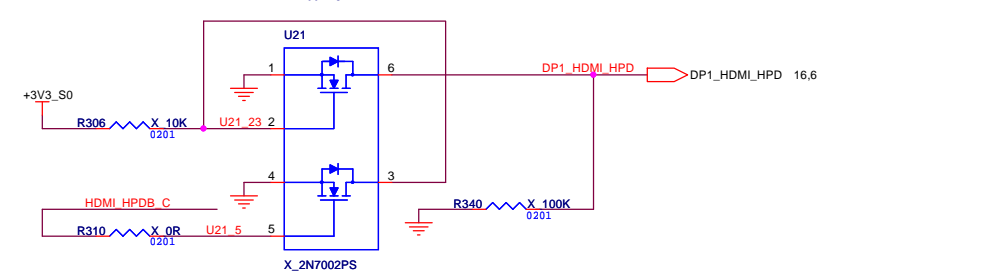
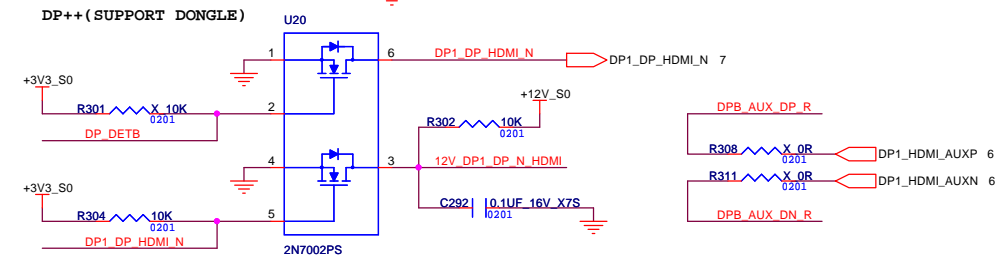
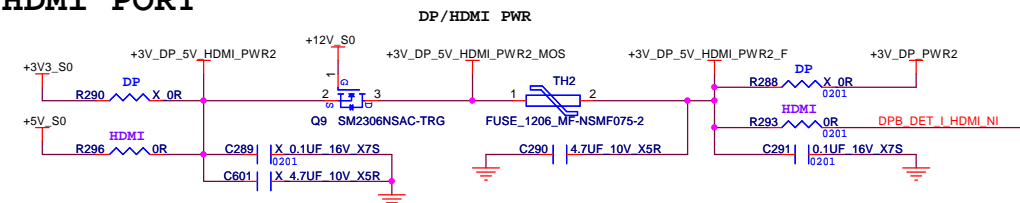
DDR4 SO-DIMM CHB



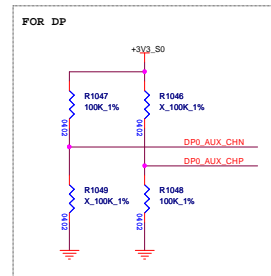
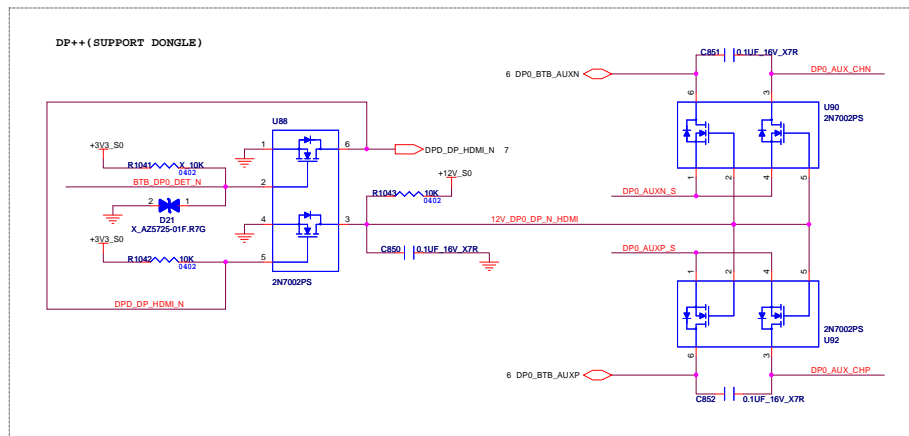
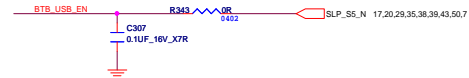
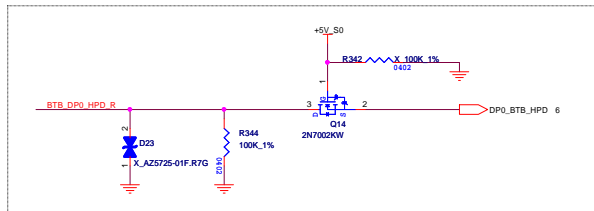
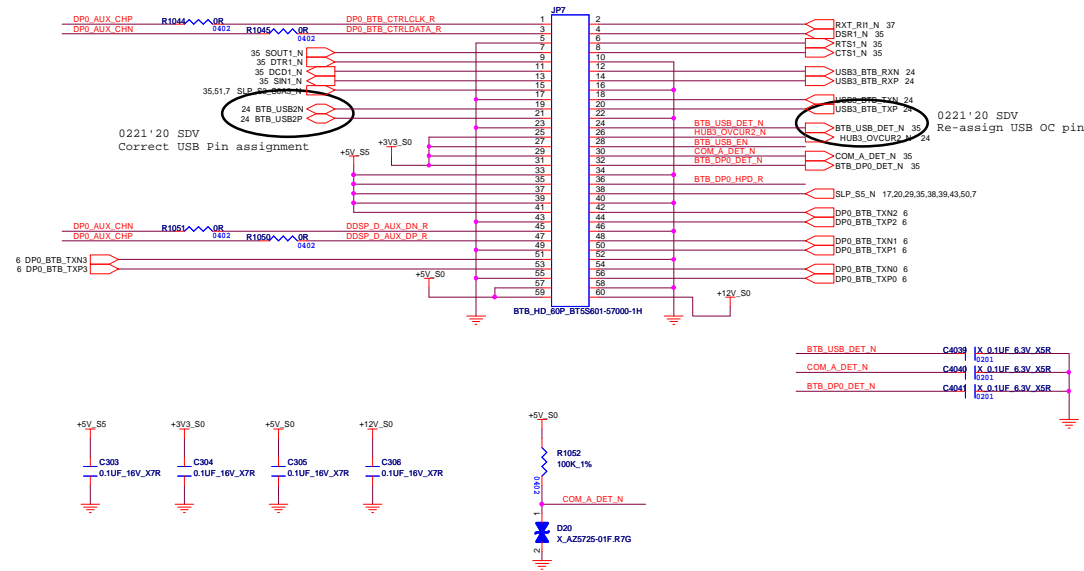
DP PORT



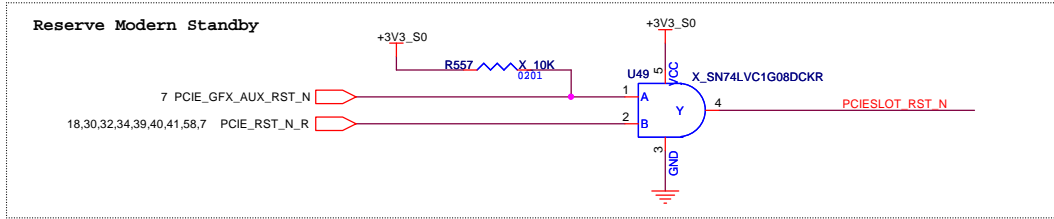
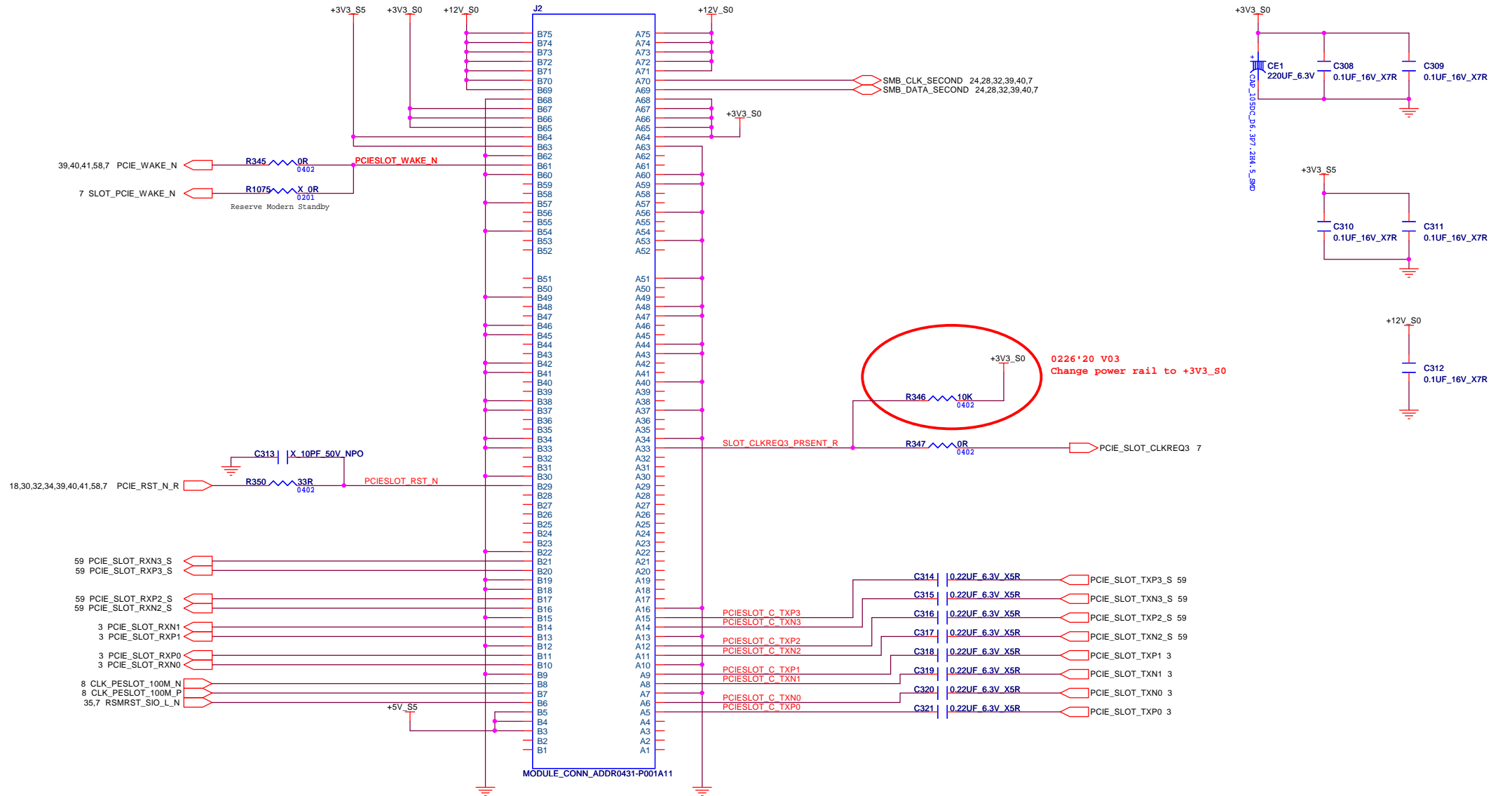
HDMI PORT



3 IN 1 BTB CONNECTOR



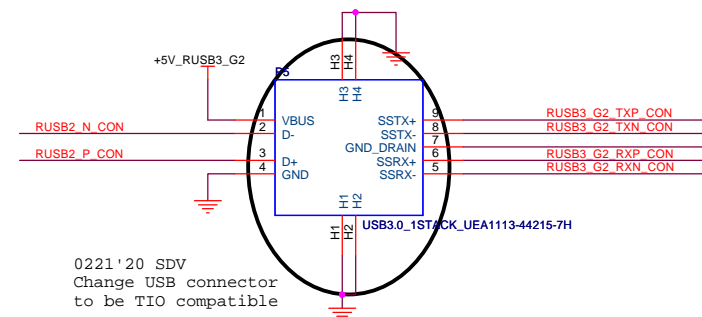
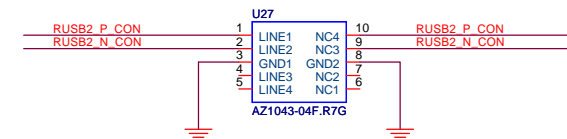
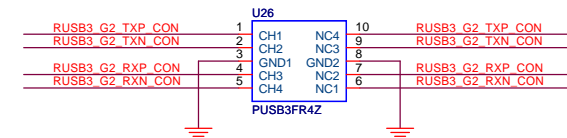
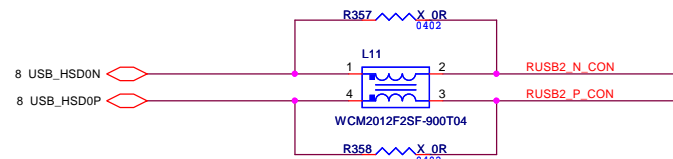
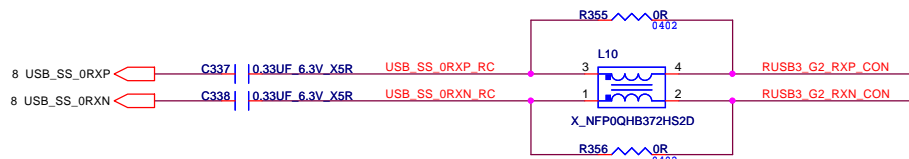
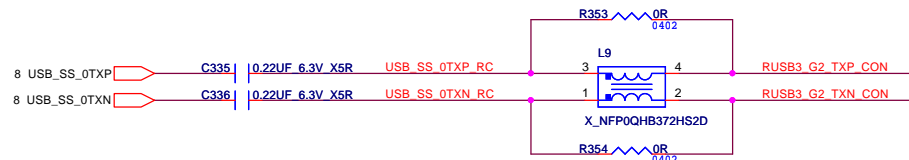
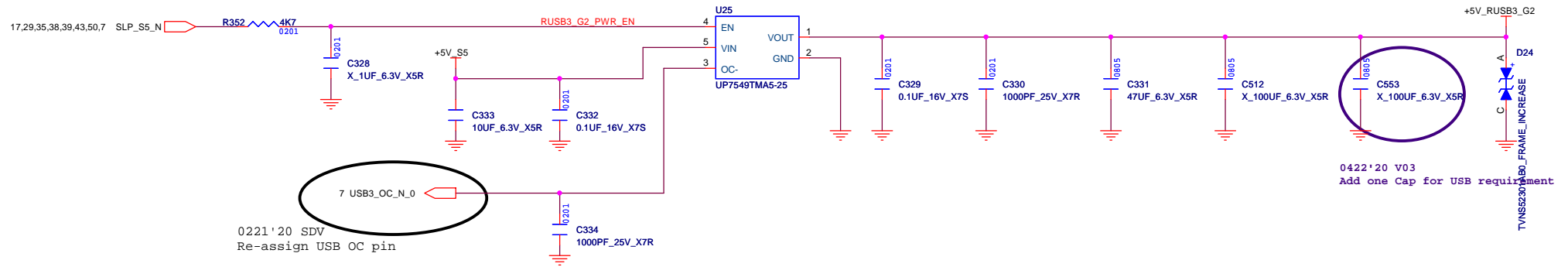
PCIE X4



A	B	C	D	E	F	G	H
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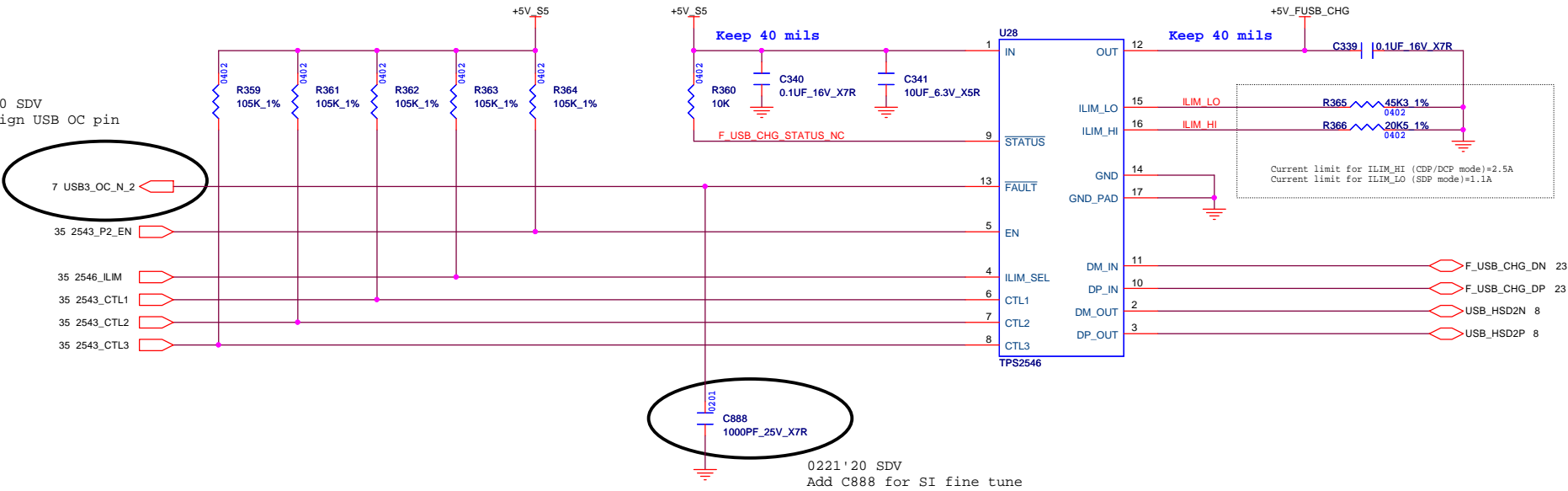


REAR USB 3.2 GEN 1 (TIO)



USB CHARGING

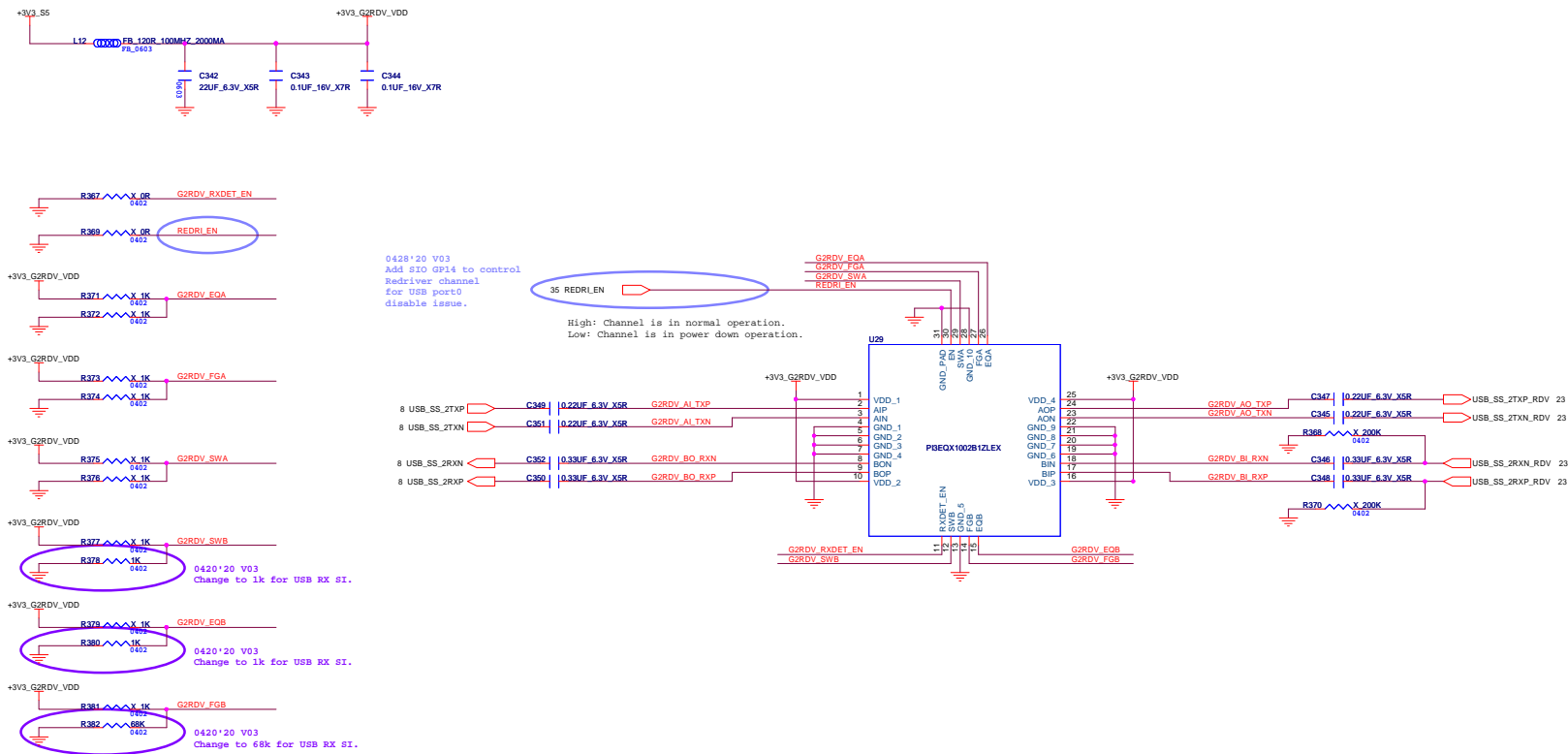
0221'20 SDV
Re-assign USB OC pin



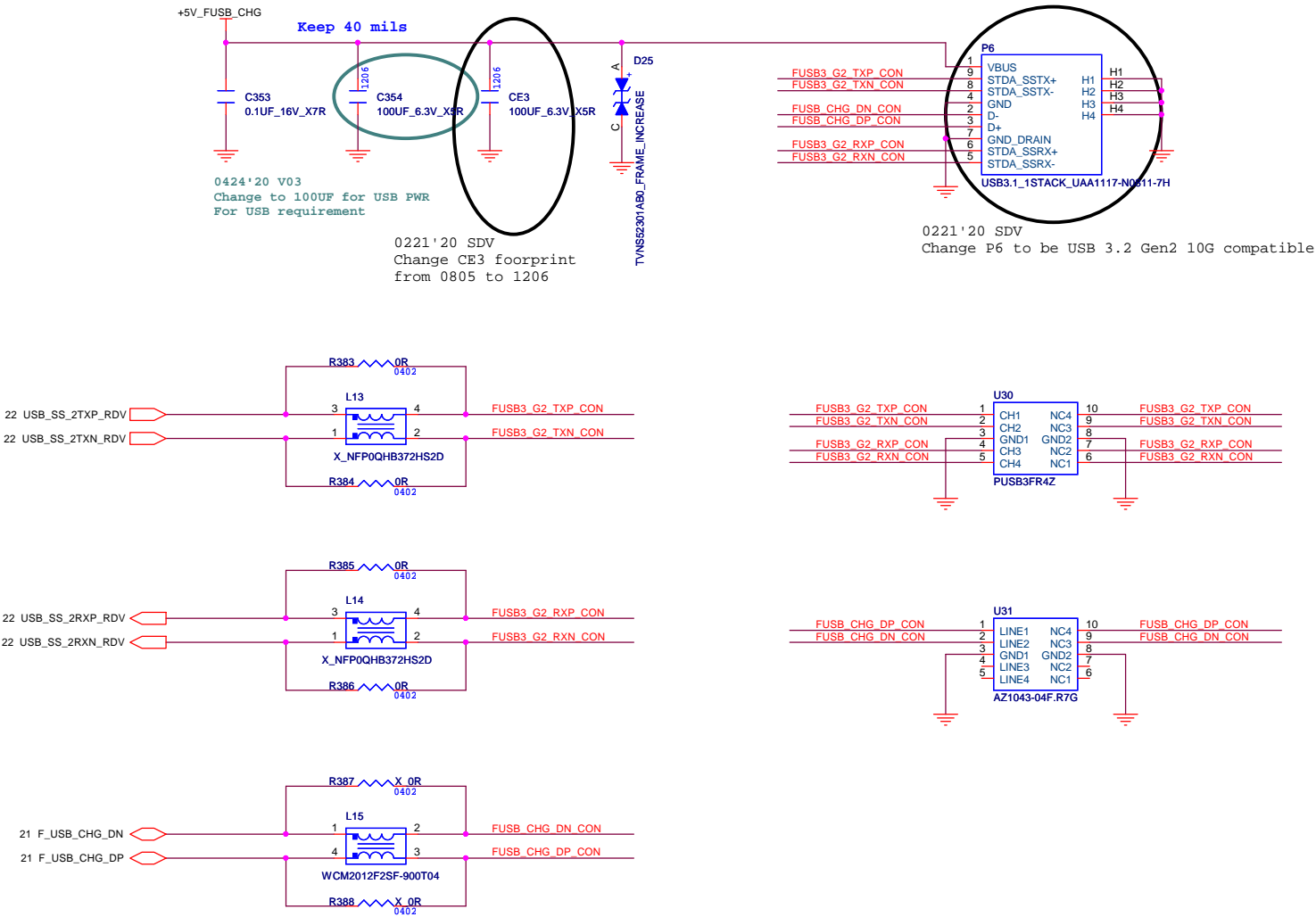
0221'20 SDV
Add C888 for SI fine tune

Control Signal			Model Select				
			CNTL1	CNTL2	CNTL3	ILIM_SEL	EN
Charge EN	S0	CDP	1	1	1	1 -ILIM_HI 2.5A	1
	S3	DCP	0	1	1	0 -ILIM_HI 2.5A	1
	S4/S5	DCP	0	0	1	1 -ILIM_HI 2.5A	1
Charge DIS	S0	SDP	0	1	0	0 -ILIM_LO 1.1A	1
	S3	SDP	0	1	0	0 -ILIM_LO 1.1A	1
	S4/S5	SDP	Shunt Down				0

USB3.1 GEN2 REDRIVER

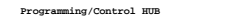
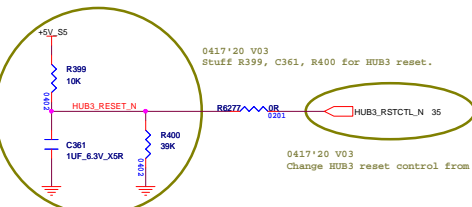


FRONT USB 3.2 GEN 2

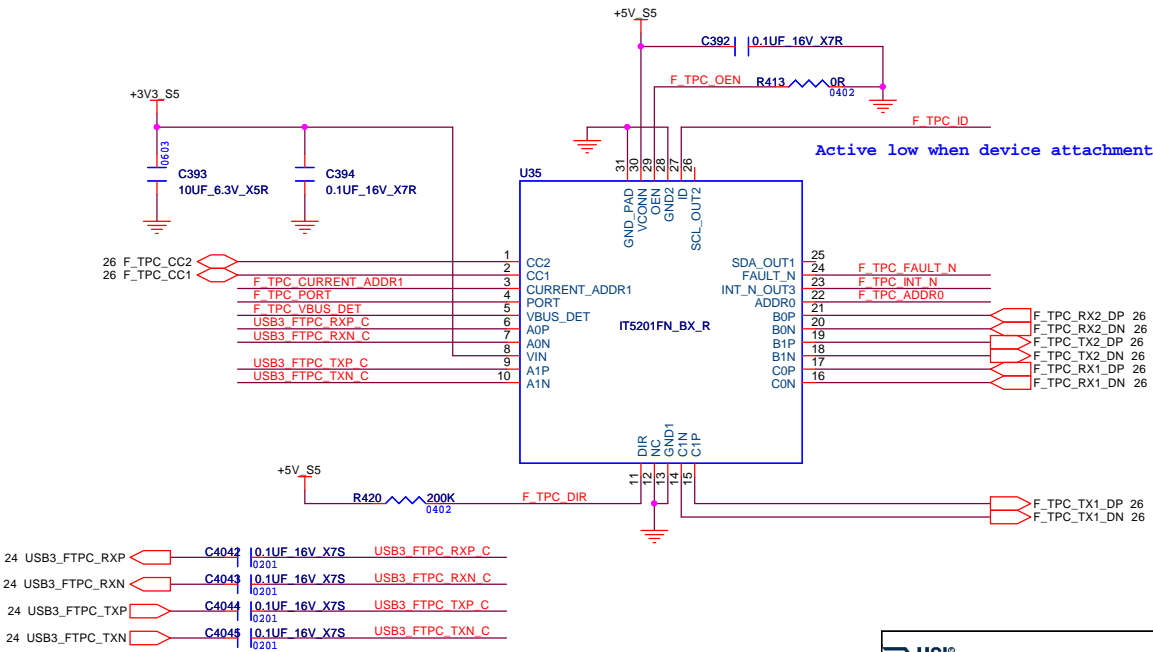
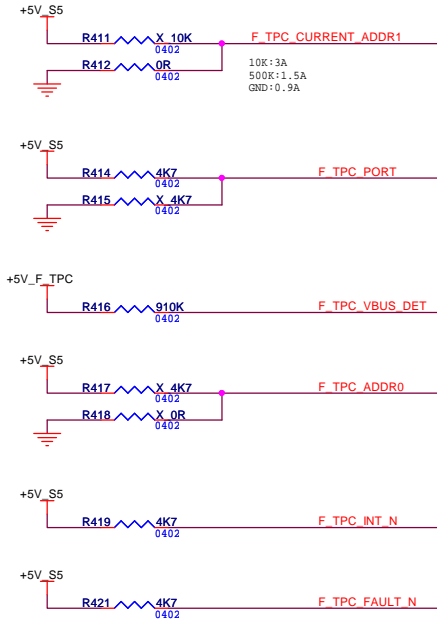
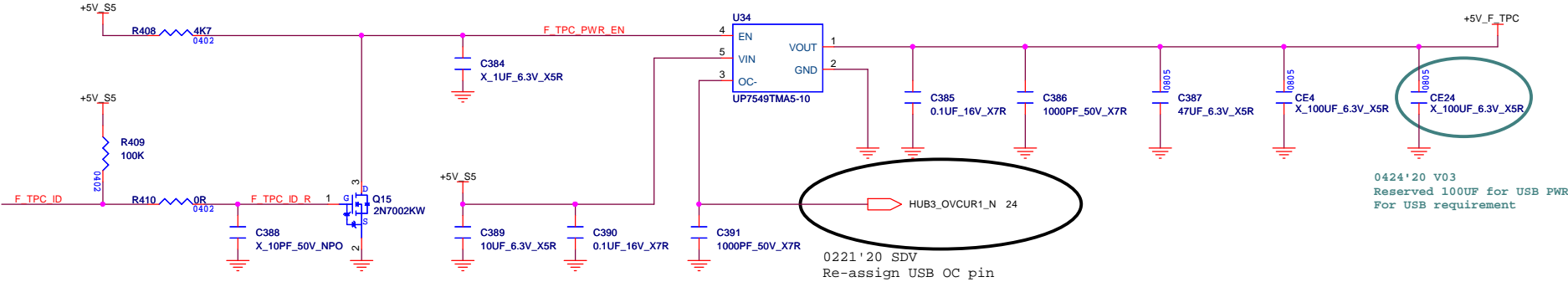


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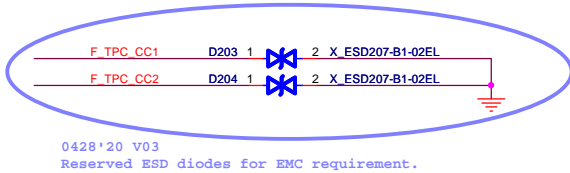
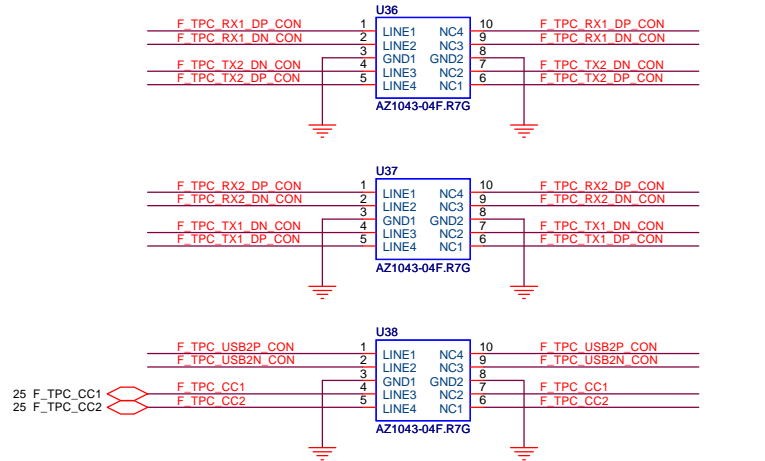
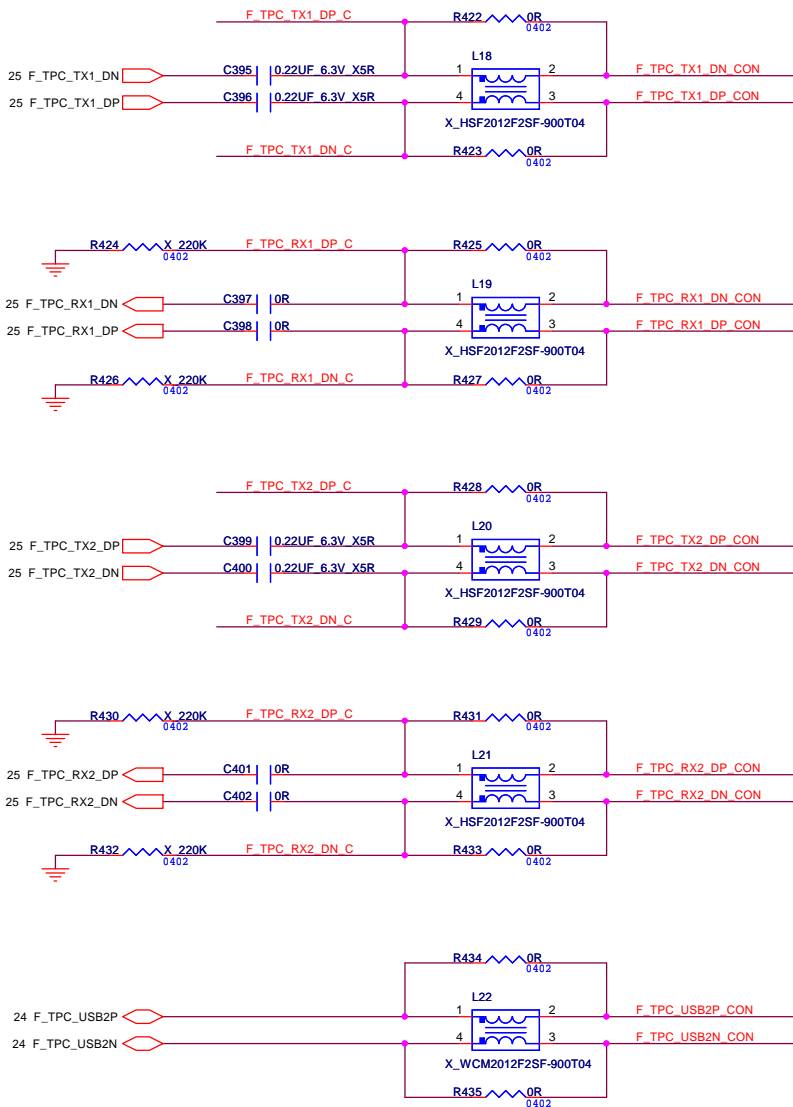
USB 3.0 HUB



TYPE C PWR & MUX

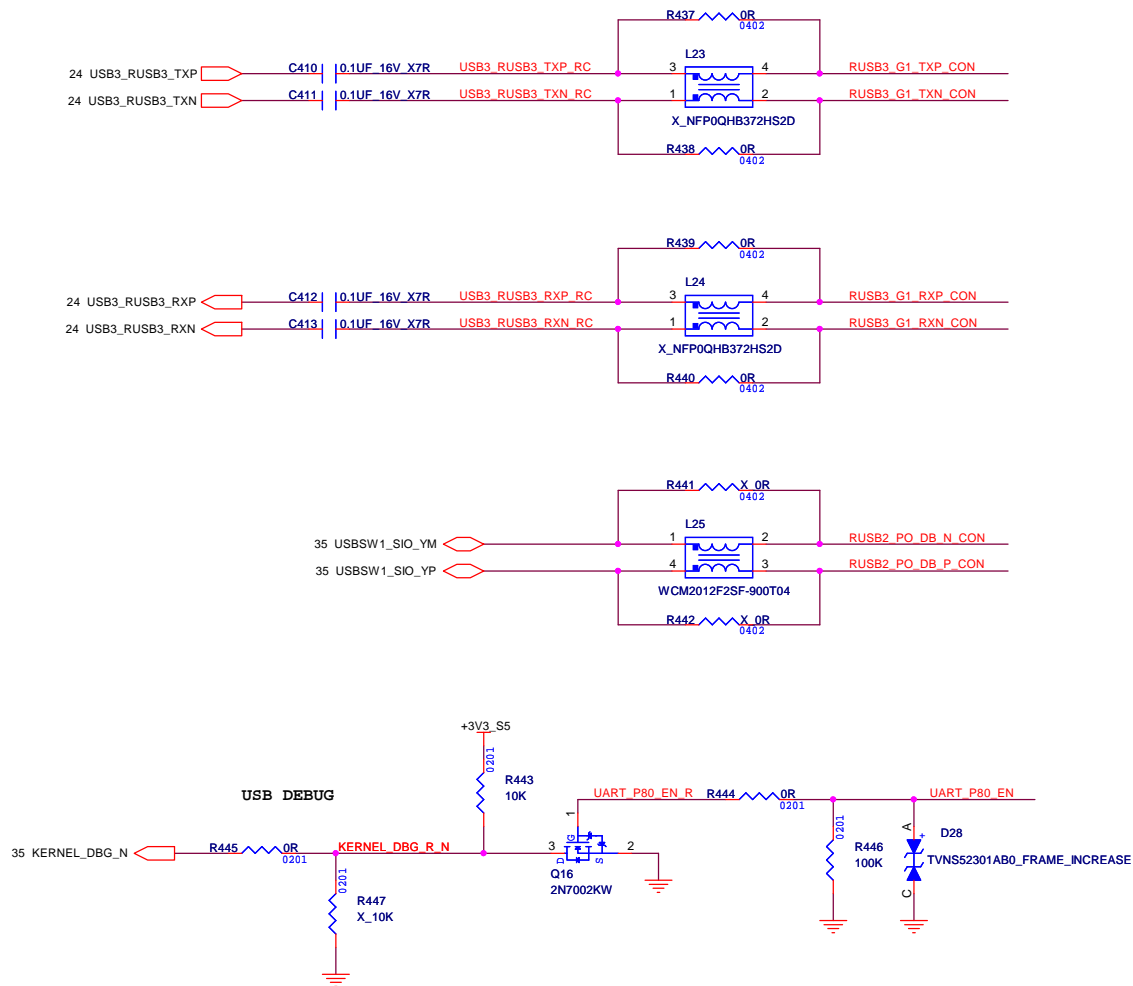
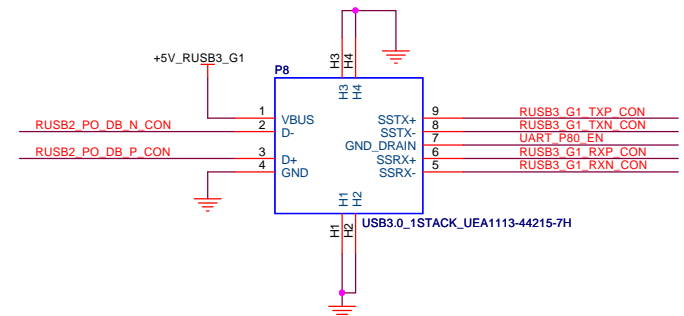


FRONT USB TYPE C PORT

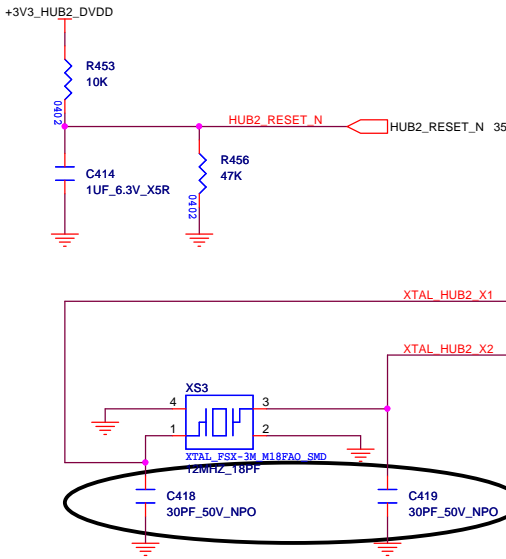
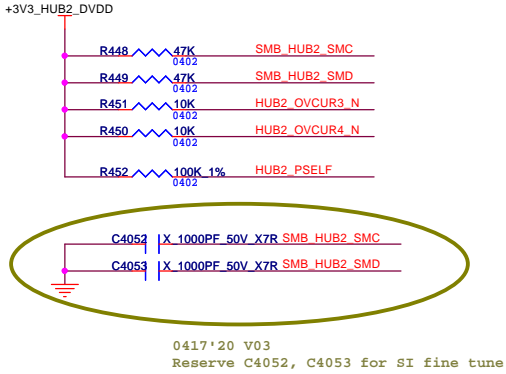


USI® Universal Scientific Industrial Co., Ltd.	
TITLE: TINY6 M75Q-2	
REV: V0.3	
Document Number: <Doc>	
Prepared by: Jason	
SIZE: A3	Date: Tuesday, April 28, 2020
PAGE: 26	of 66

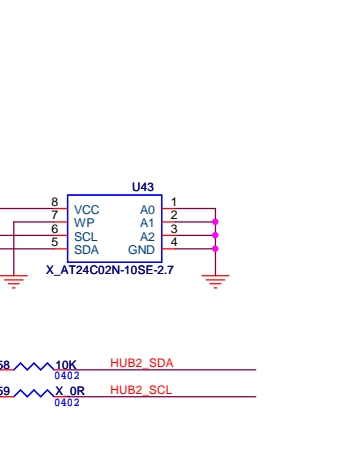
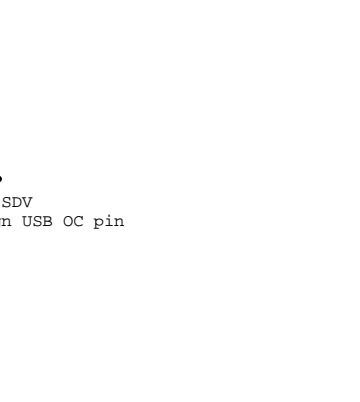
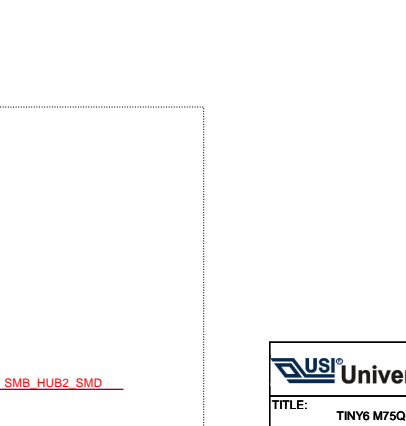
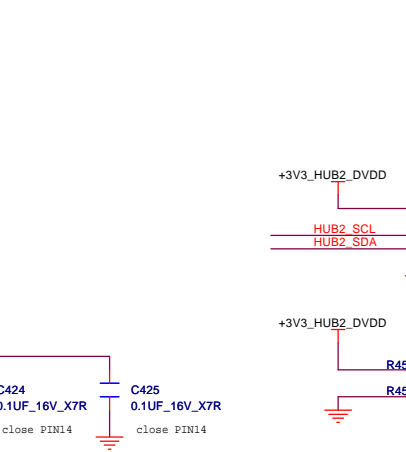
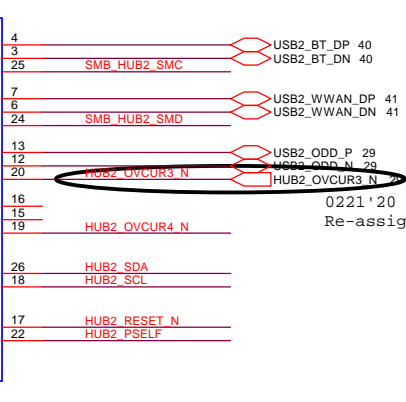
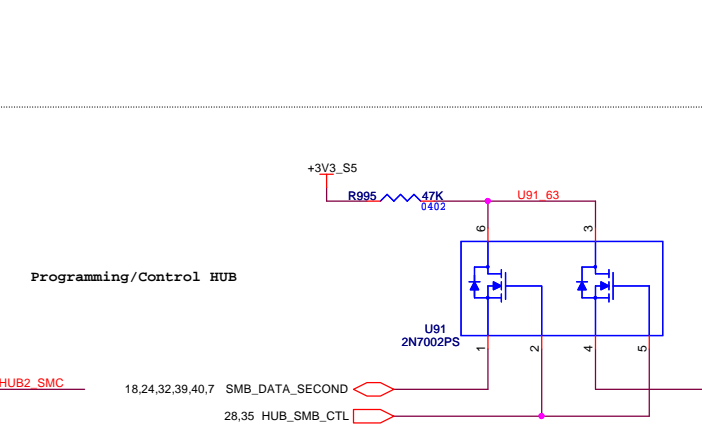
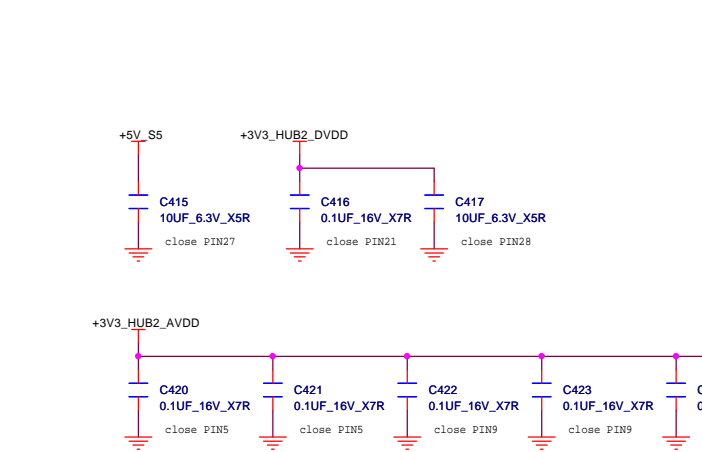
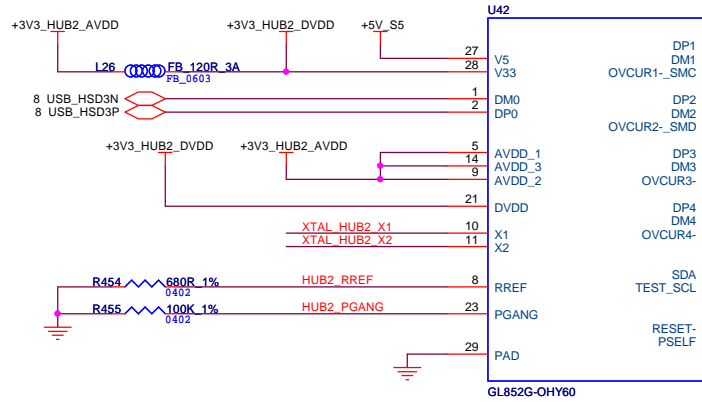
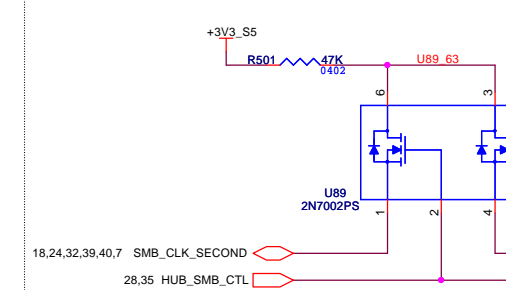
USB POWER ON & DEBUG



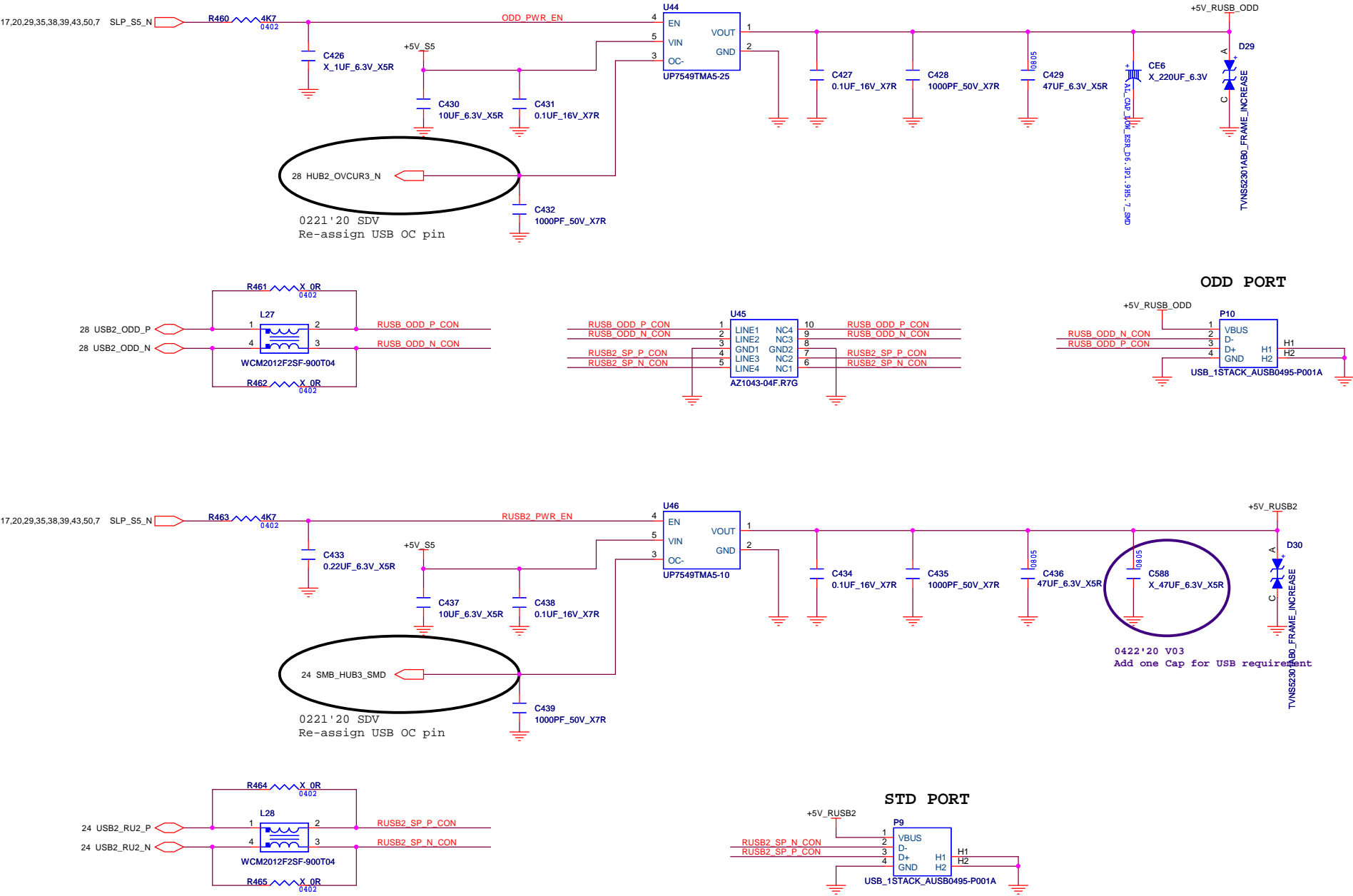
USB 2.0 HUB



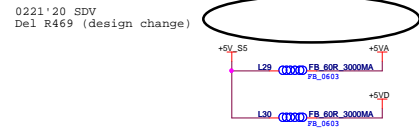
0221'20 SDV
Change C418/C419 from 18pF to 30pF
for better accuracy



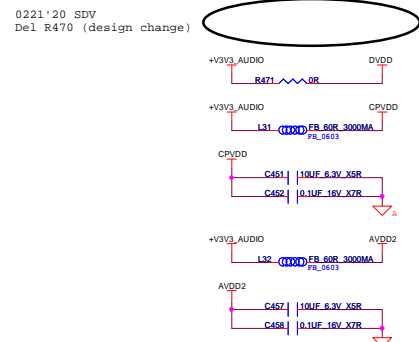
REAR USB 2.0 PORTS



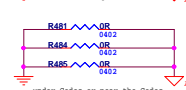
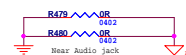
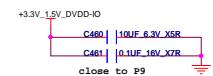
AUDIO CODEC ALC222



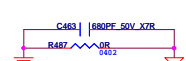
0221'20 SDV
Del R469 (design change)



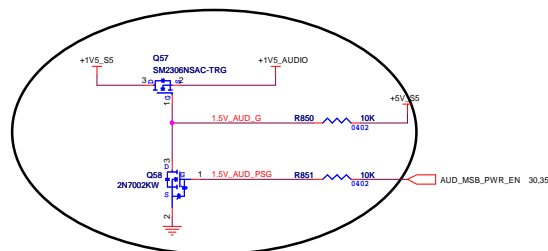
0221'20 SDV
Del R470 (design change)



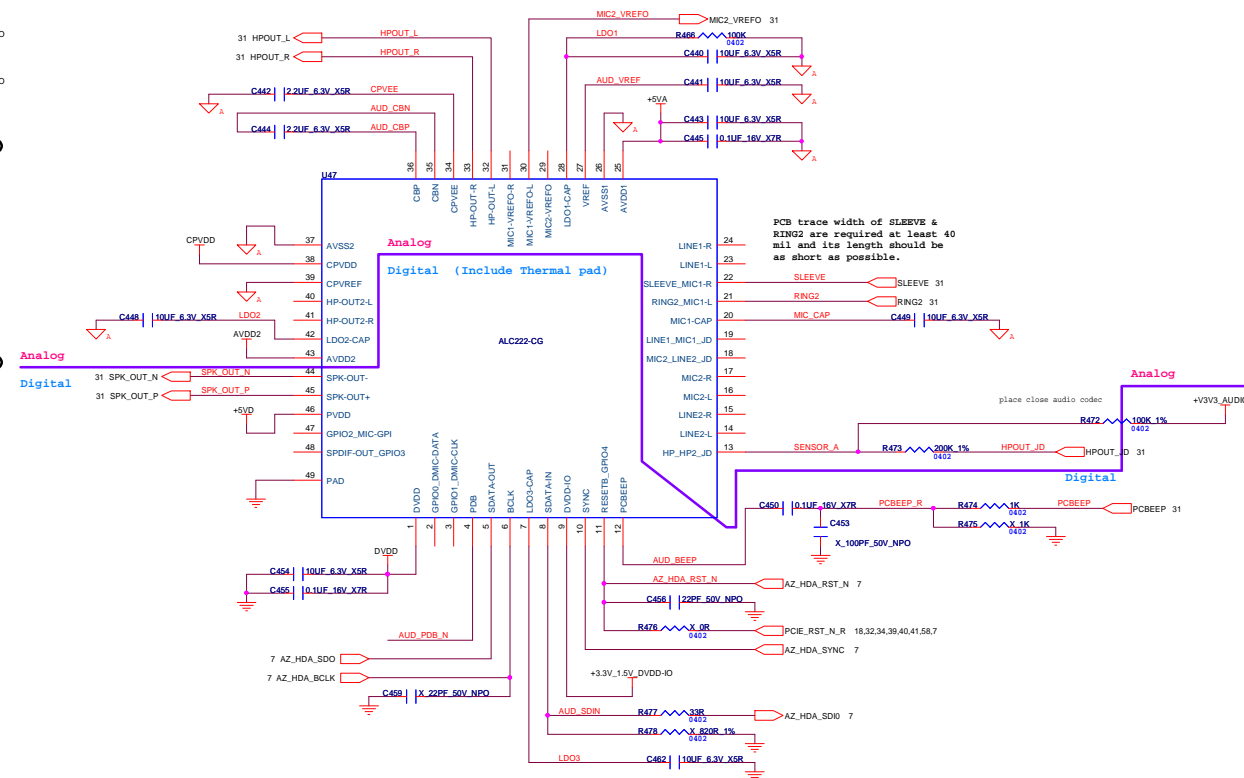
under Codec or near the Codec



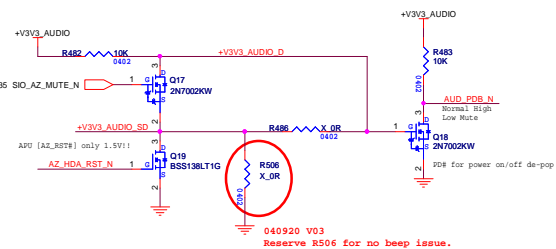
Near AVDD1 and AVDD2 power source input



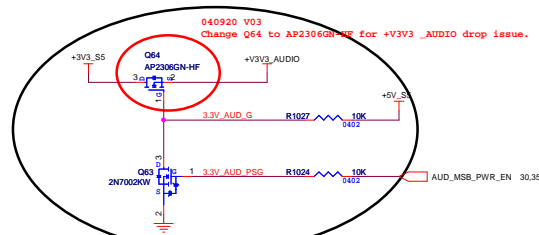
```
0221'20 SDV
Move page
Change R851 control from PSON_N to AUD_MSB_PWR_EN
```



PCB trace width of SLEEVE & RING2 are required at least 4 mil and its length should be as short as possible.

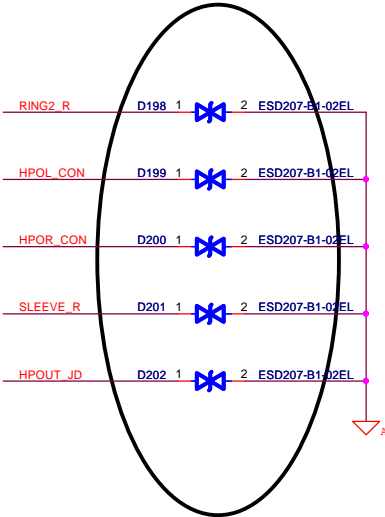
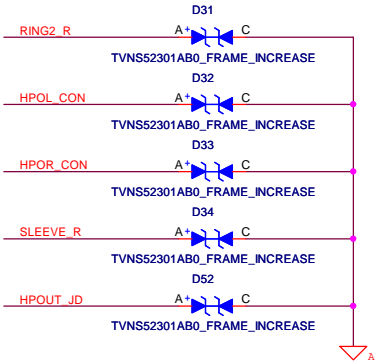
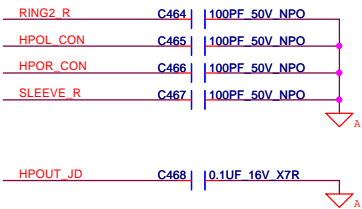
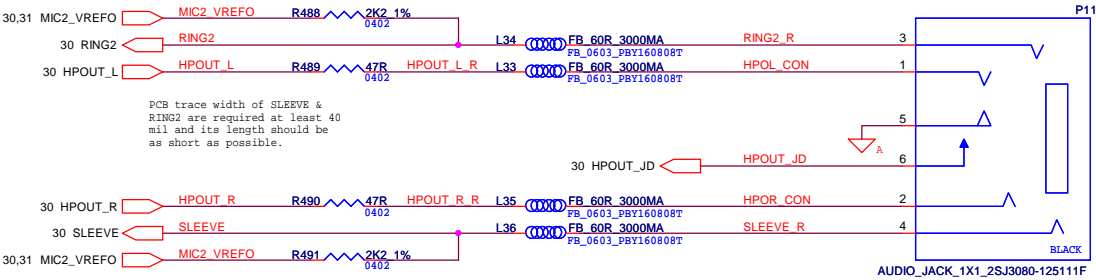


040920 V03
Reserve R506 for no beep issue.

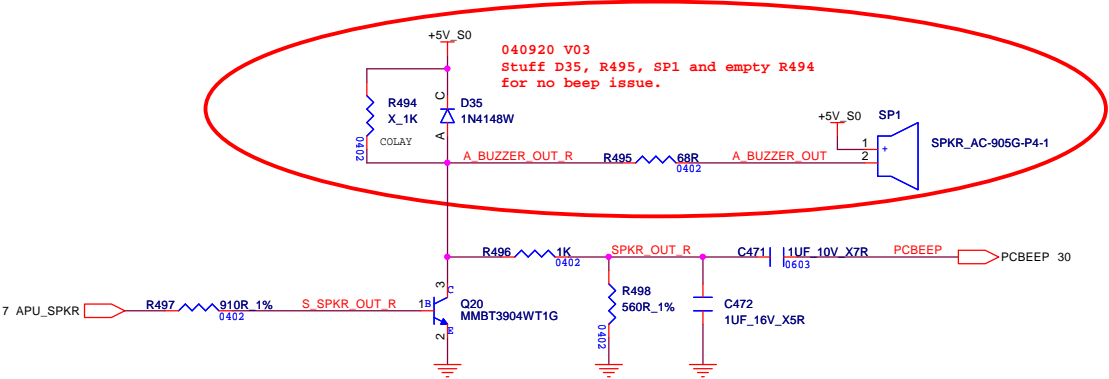
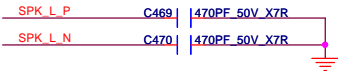
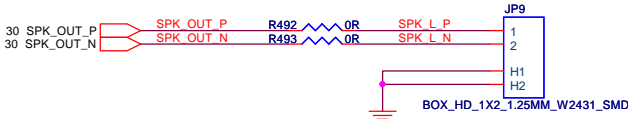


0221'20 SDV
Modify the +V3V3_AUDIO control to be Modern Standby Ready
Add Q63/Q64
Re-assign R1024/R1027

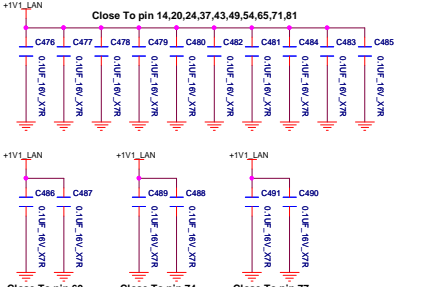
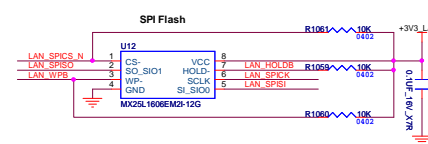
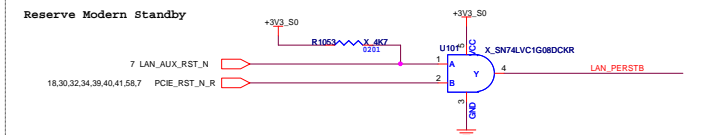
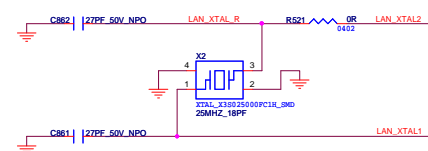
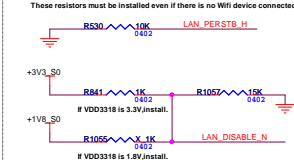
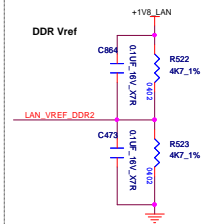
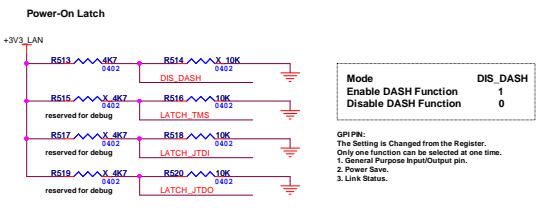
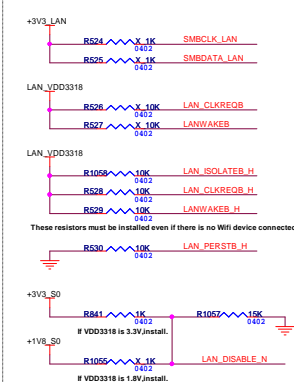
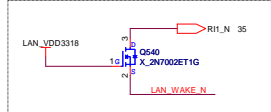
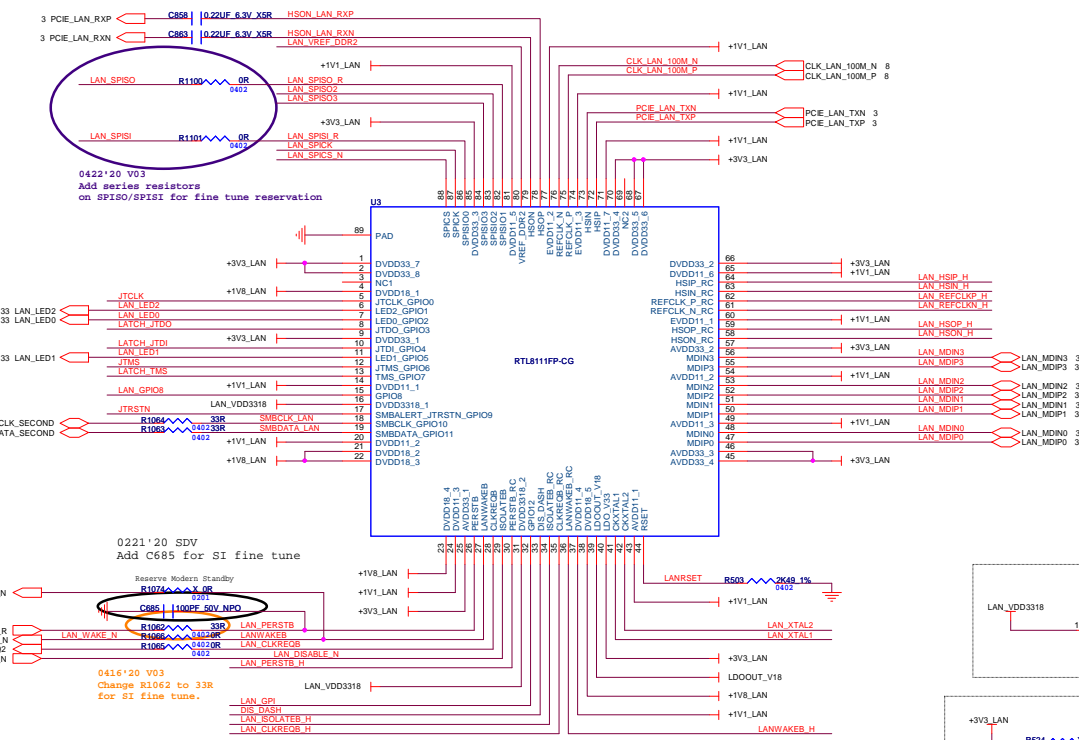
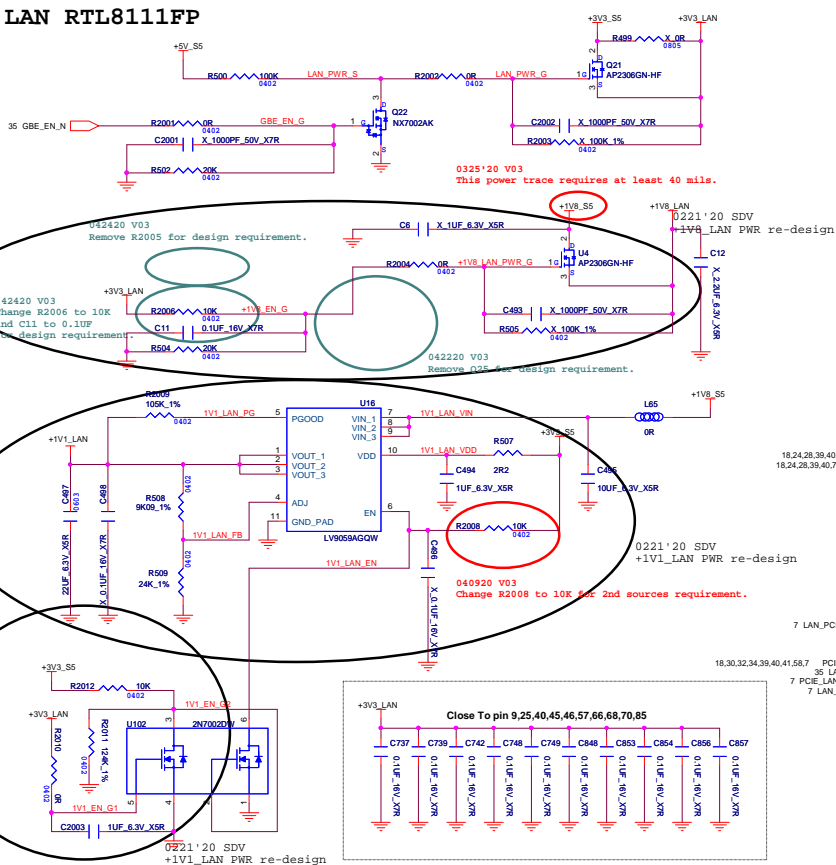
AUDIO JACK & SPK & BUZZER



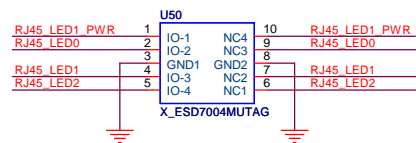
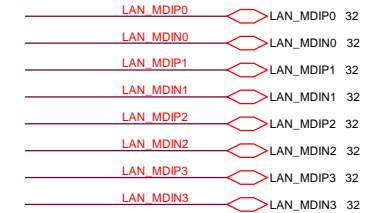
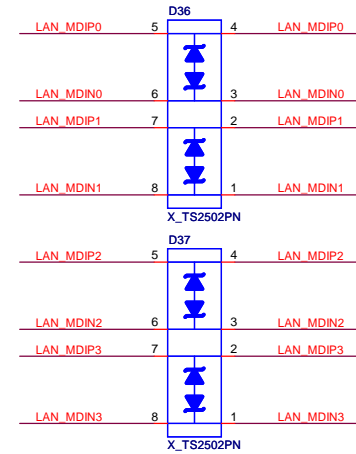
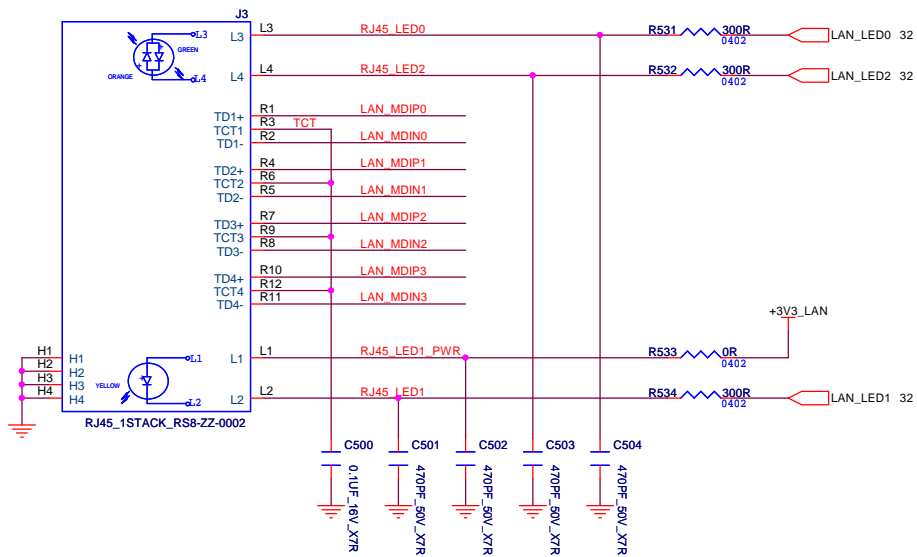
0221'20 SDV
Add D198/D199/D200/D201/D202 for ESD consideration



LAN RTL8111FP

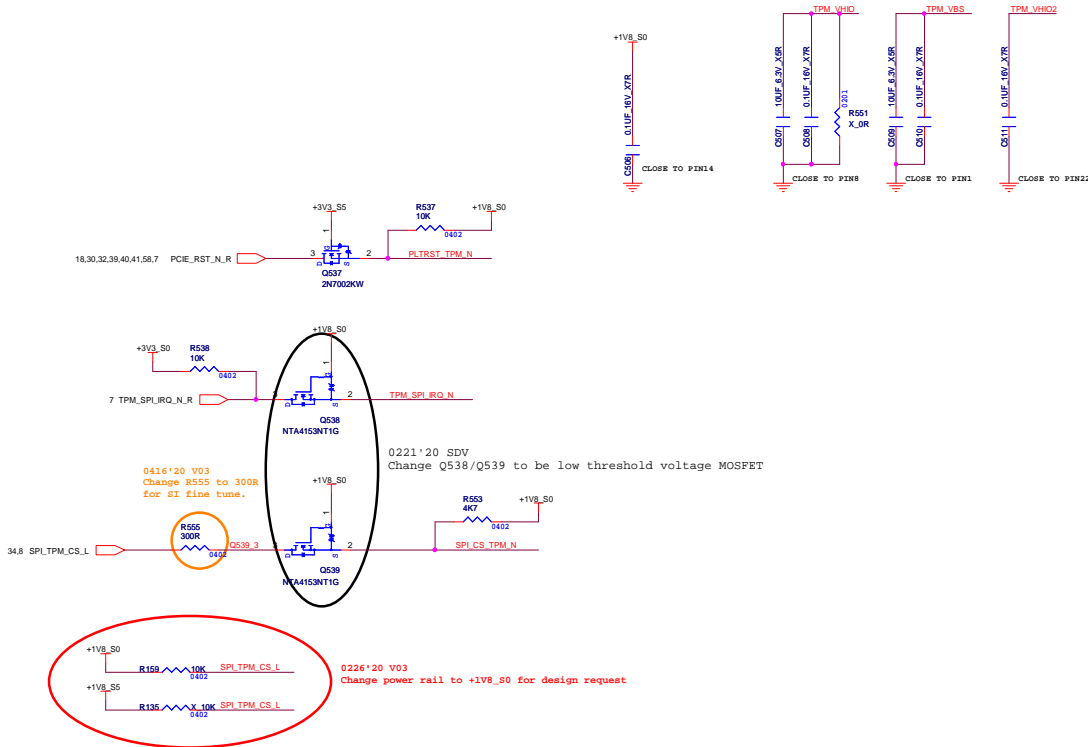
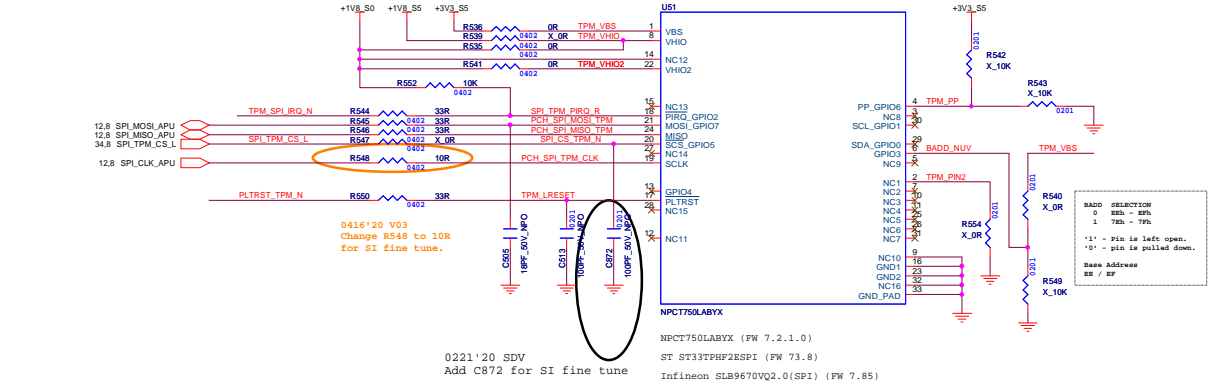


RJ45 CONNECTOR



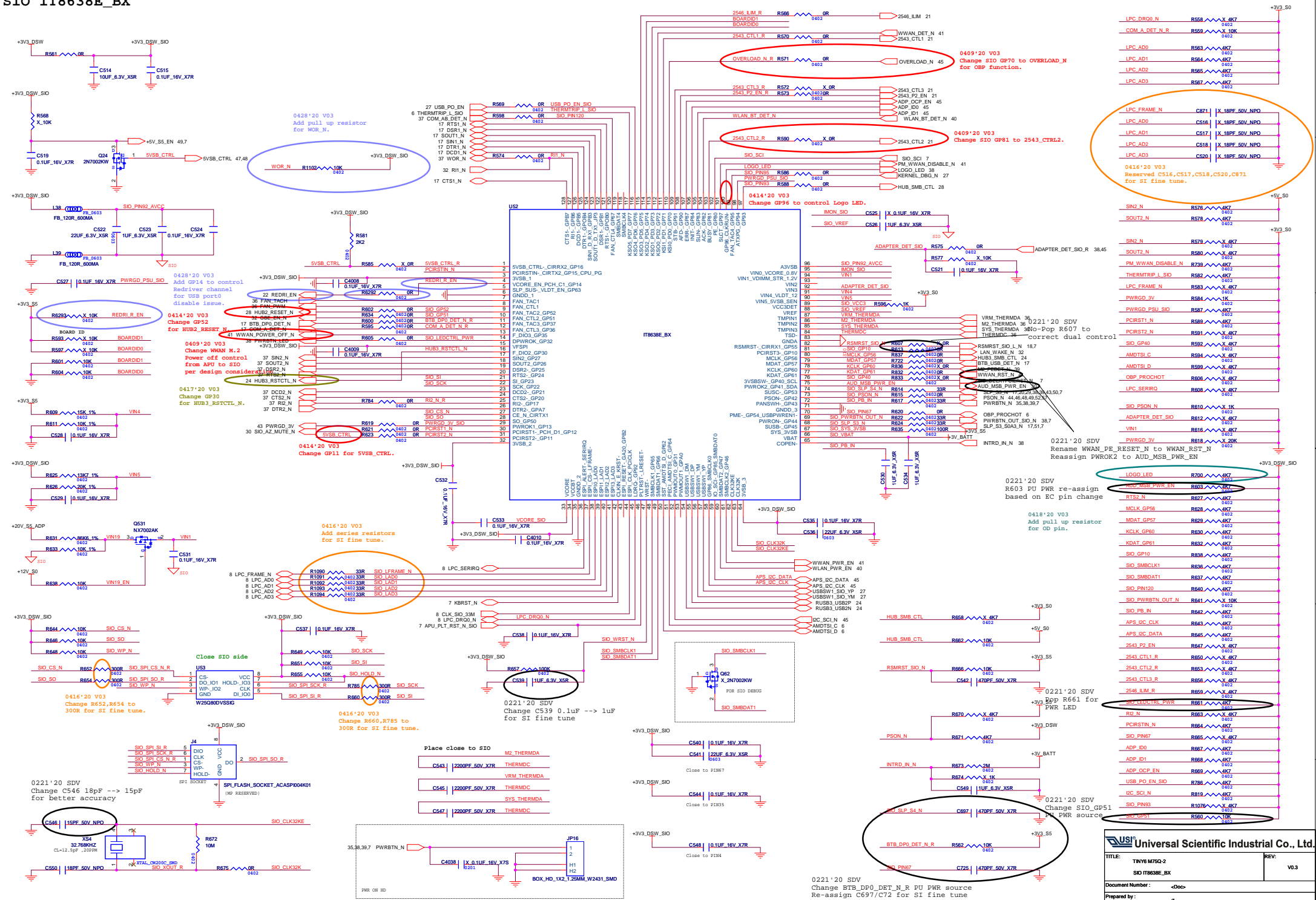
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SPI TPM

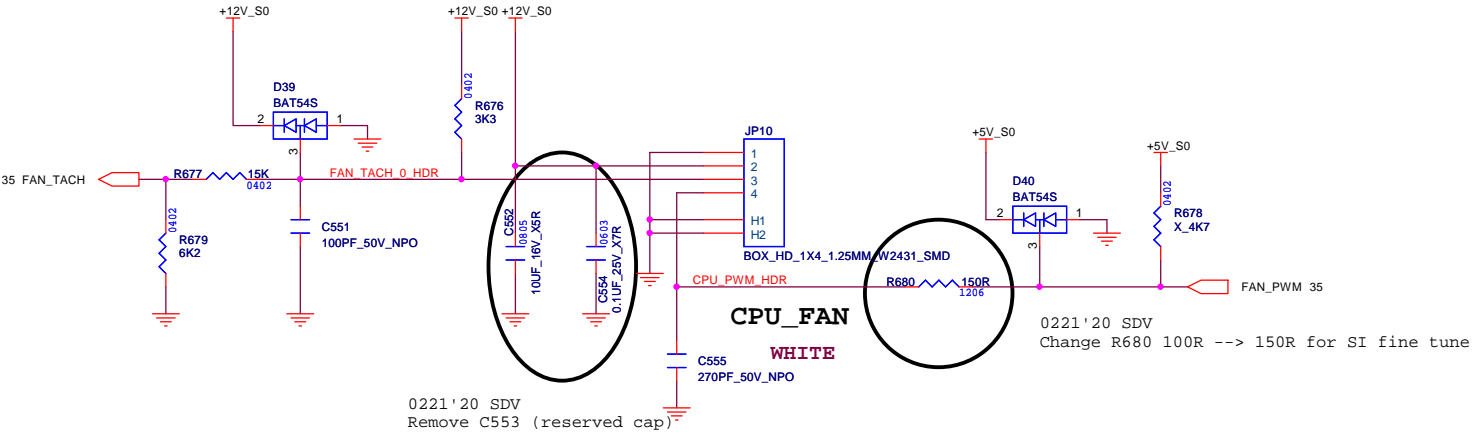


	INF	ST	NUVO
PIN1	VDD	NC	VSB
PIN2	GND	GND	NC_2
PIN3	NC	NC	GPIO/GPIO2
PIN4	NC	NC	PP
PIN5	NC	NC	TEST
PIN6	GPIO	NC	GPIO3/BADD
PIN7	PP	PP	NC_7
PIN8	GND	NC	VDD_8
PIN9	NC	NC	GND_9
PIN10	NC	NC	NC_9
PIN11	NC	NC	NC_10
PIN12	NC	NC	NC_11
PIN13	NC	NC	CLKRUNG/HQ4/SINT
PIN14	NC	NC	VHIO
PIN15	NC	NC	LAD3
PIN16	NC	NC	GND_16
PIN17	RST#	SPI_RST	SPI_RST
PIN18	PIRQ#	SPI_PIRQ	LAD2/SPI_IRQ
PIN19	SCLK	SPI_CLK	LCLK/SCLK
PIN20	CS#	SPI_CS	LFRAME/CS
PIN21	MOST	MOST	LAD1/MOST
PIN22	VDD	VPS	VHIO_22
PIN23	GND	NC	GND_23
PIN24	MISO	MISO	LAD0/MISO
PIN25	NC	NC	NC
PIN26	NC	NC	NC
PIN27	NC	NC	SERIRQ
PIN28	NC	NC	LPCCPD
PIN29	NC	NC	SDA/GPIO0
PIN30	NC	NC	GPIO1/SCL
PIN31	NC	NC	NC
PIN32	GND	NC	GND

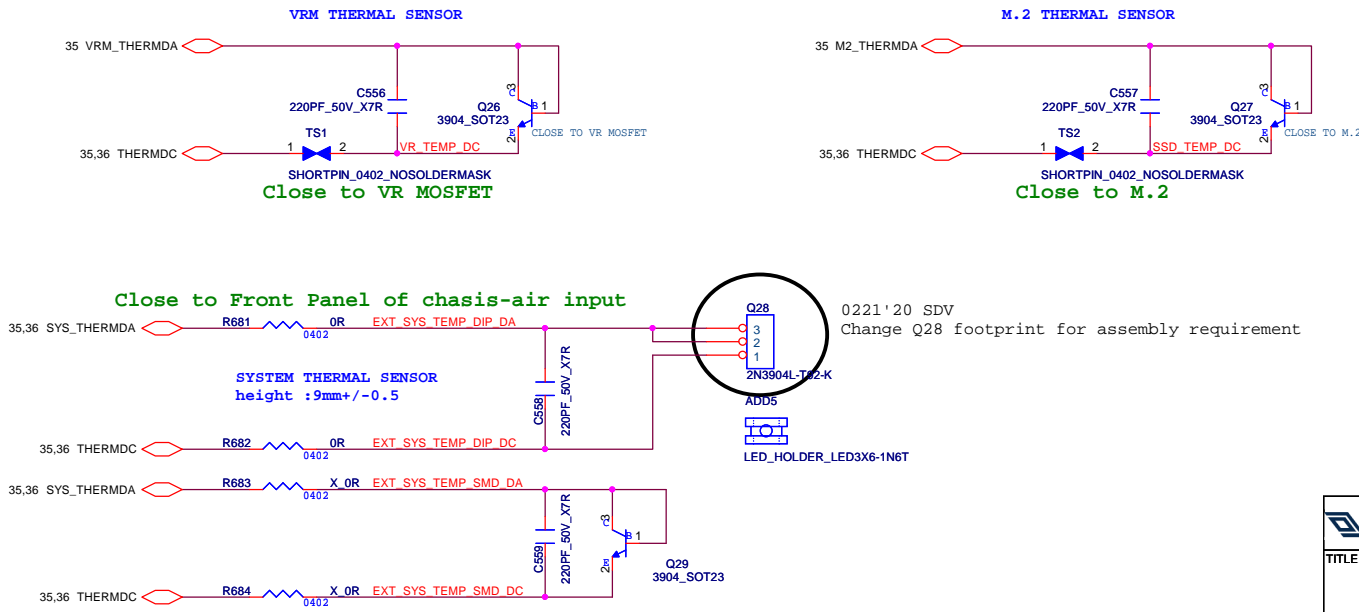
SIO IT8638E_BX



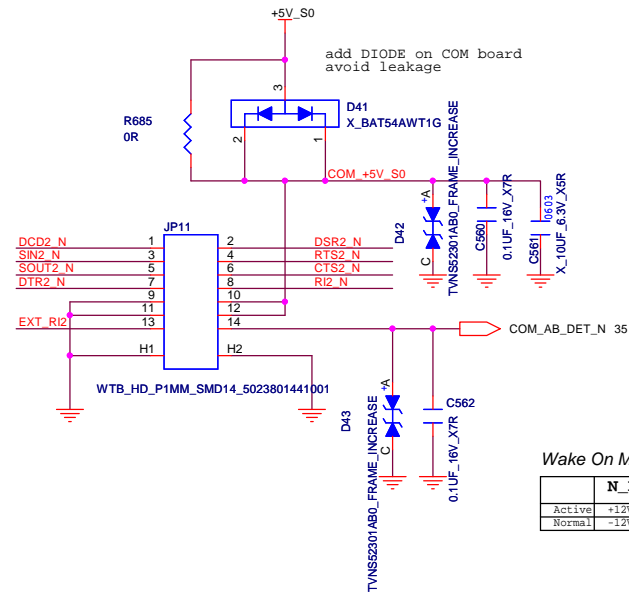
CPU FAN



THERMAL SENSOR

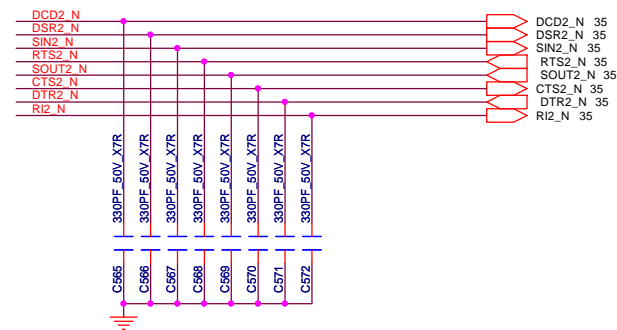
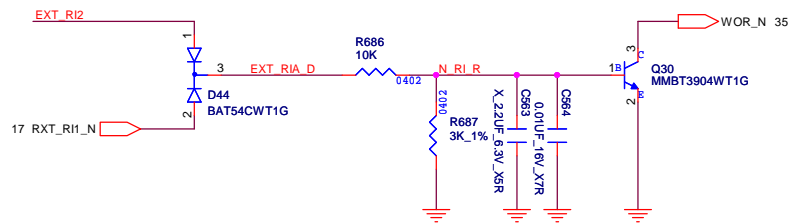


COM PORT

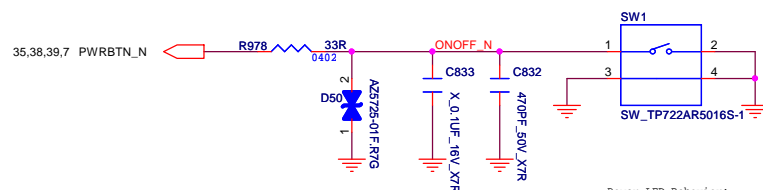
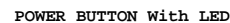
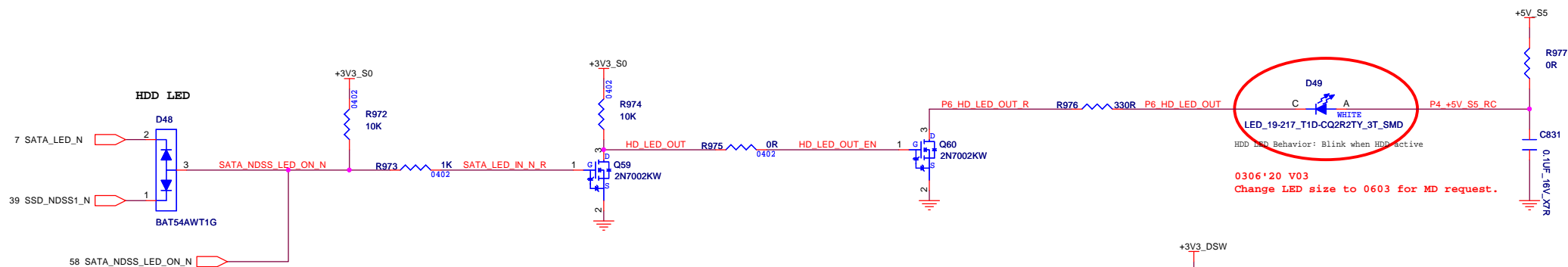


Wake On Modem Header

	N_RI	RI#
Active	+12V_S0	Low
Normal	-12V	High



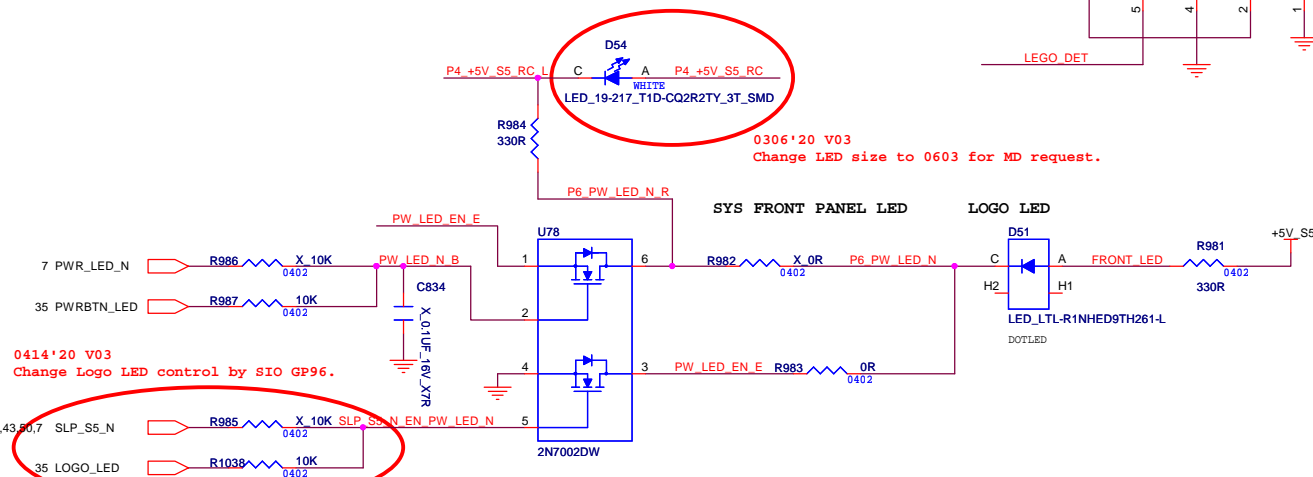
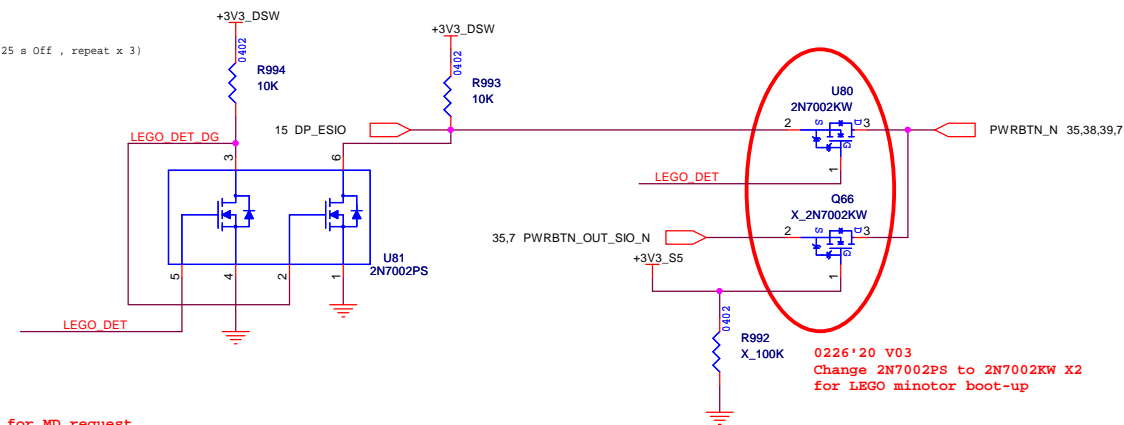
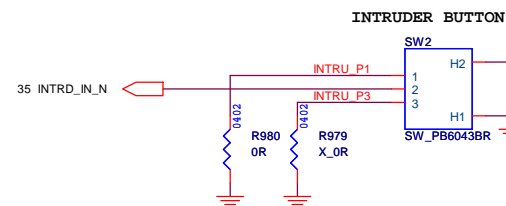
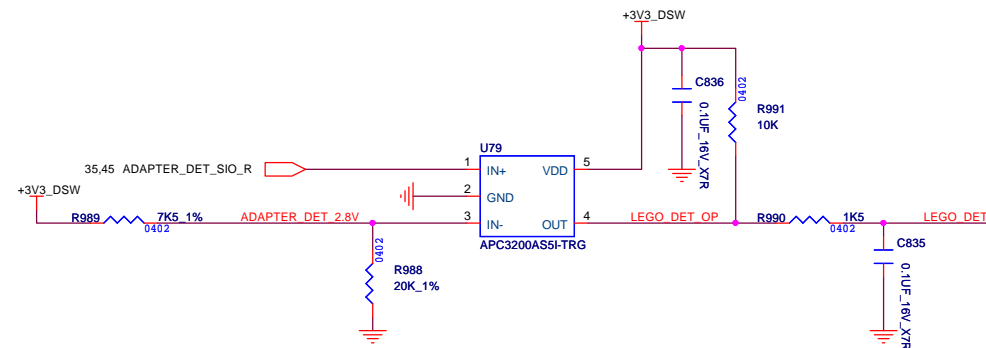
CONTROL PANEL & LED



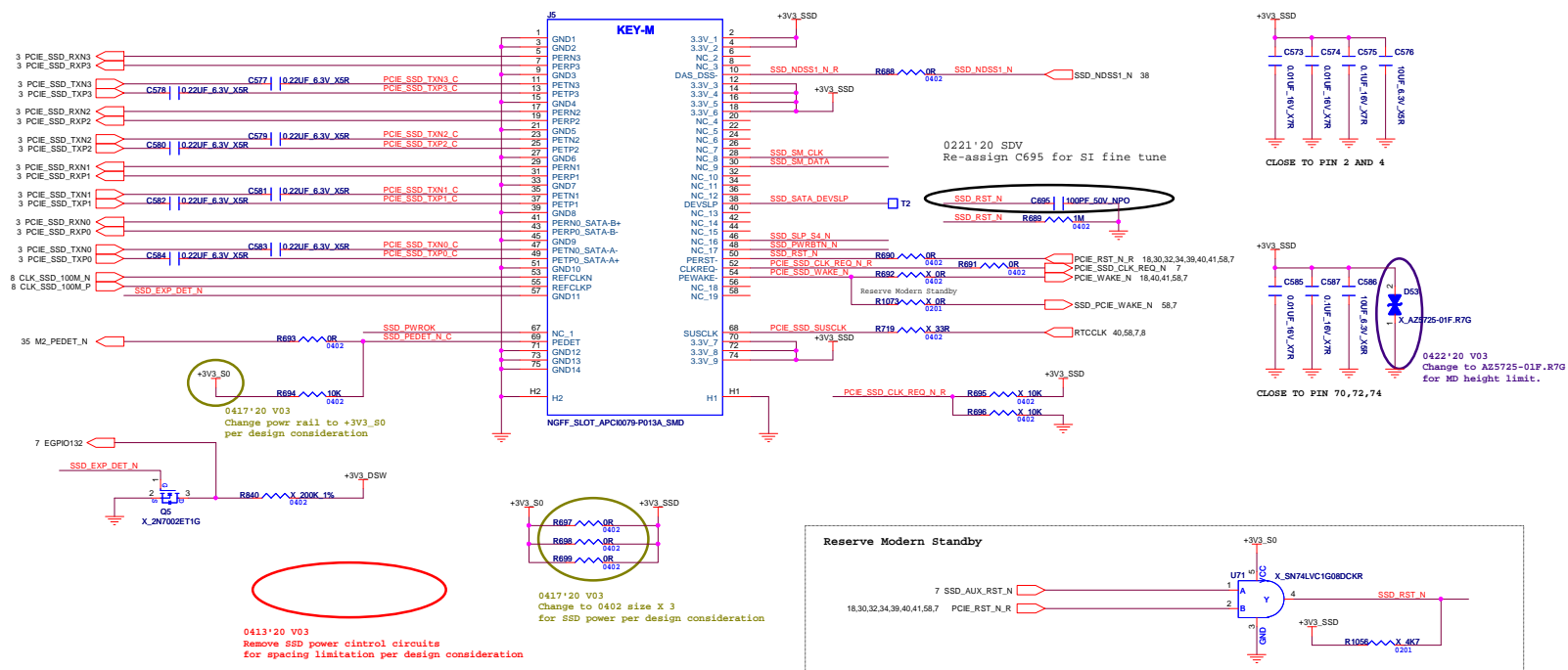
```

Power LED Behavior:
- System on: On
- System in Standby
Gradual is On, Gradual is OFF, 3s OFF
- Initial Connection of Power
(e.g. via AC adaptor or AC-in) Blink 3 Times (0.25 s On/ 0.25 s Off , repeat x 3)
- System entering hibernation Blink (0.25 s On/ 0.25 s Off)
- System off OFF

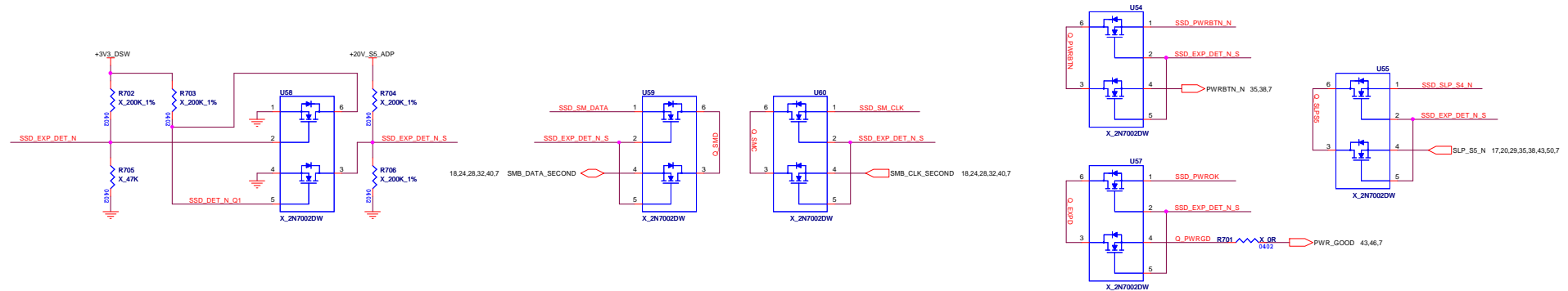
```



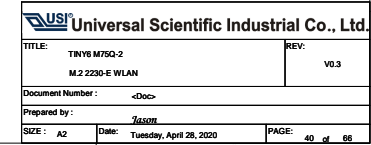
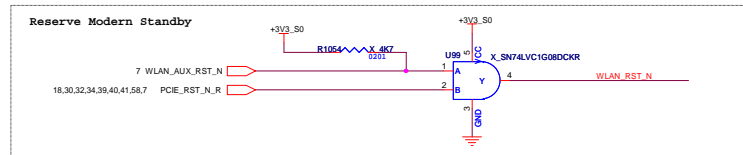
M.2 2280-M SSD

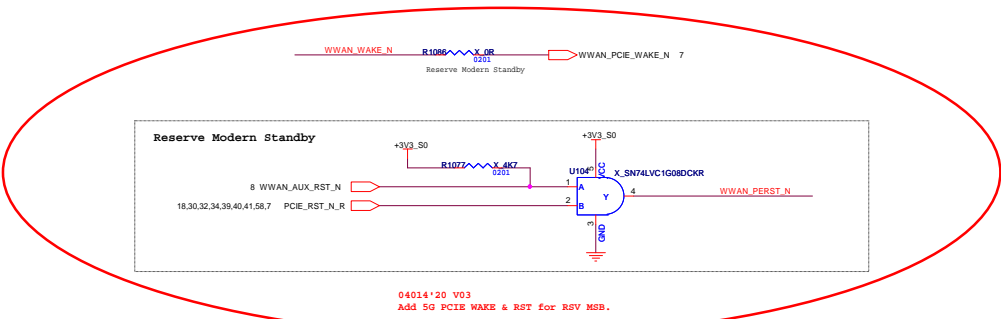
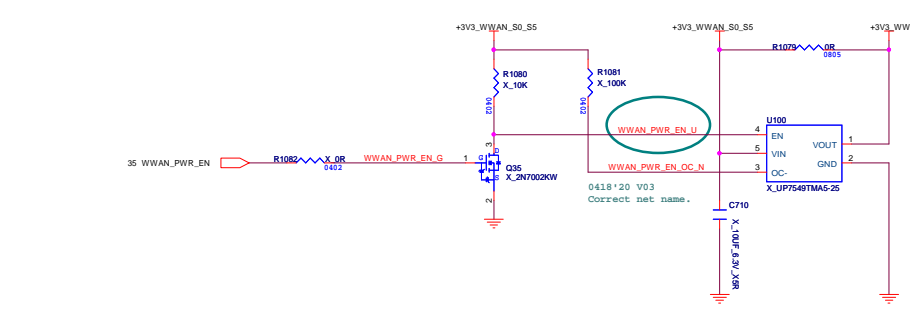
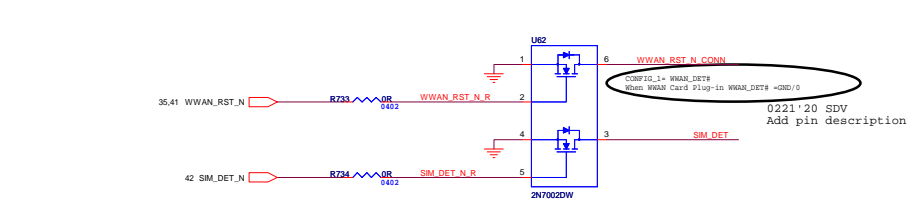
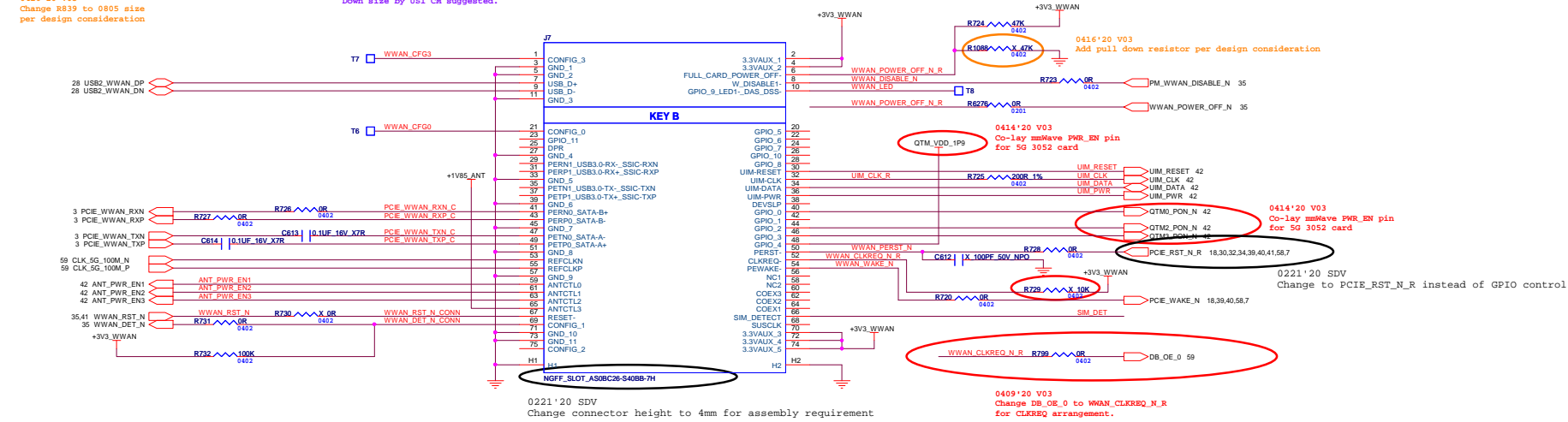
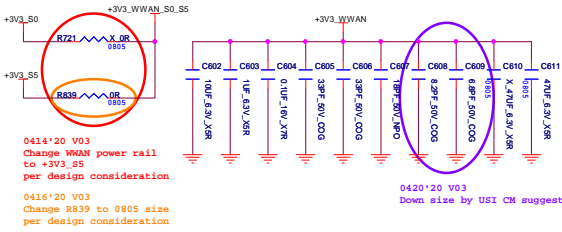


Support MOD

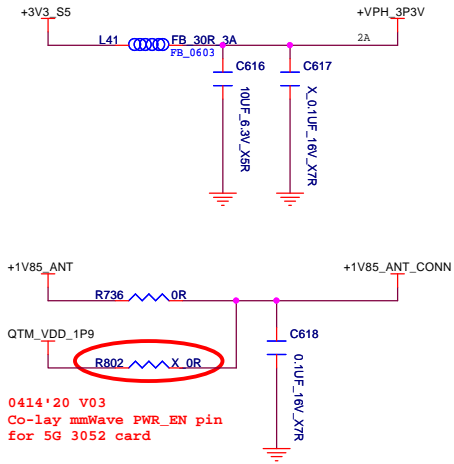
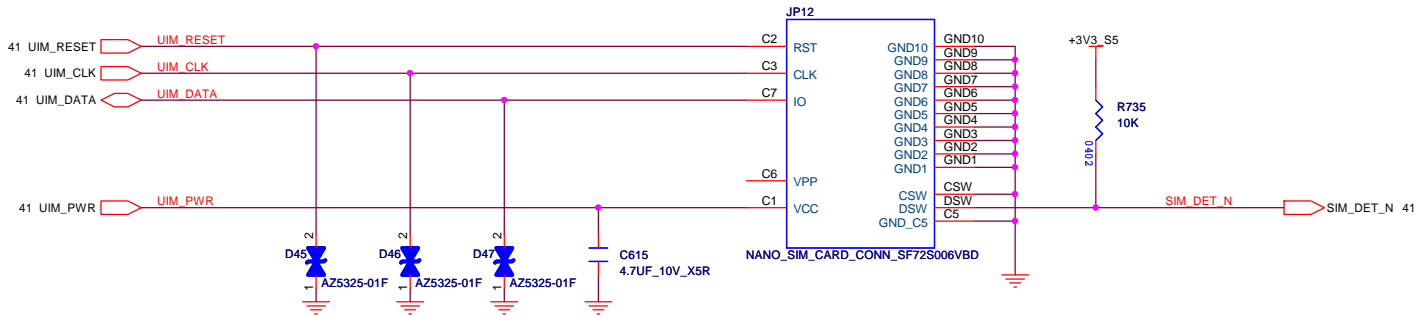


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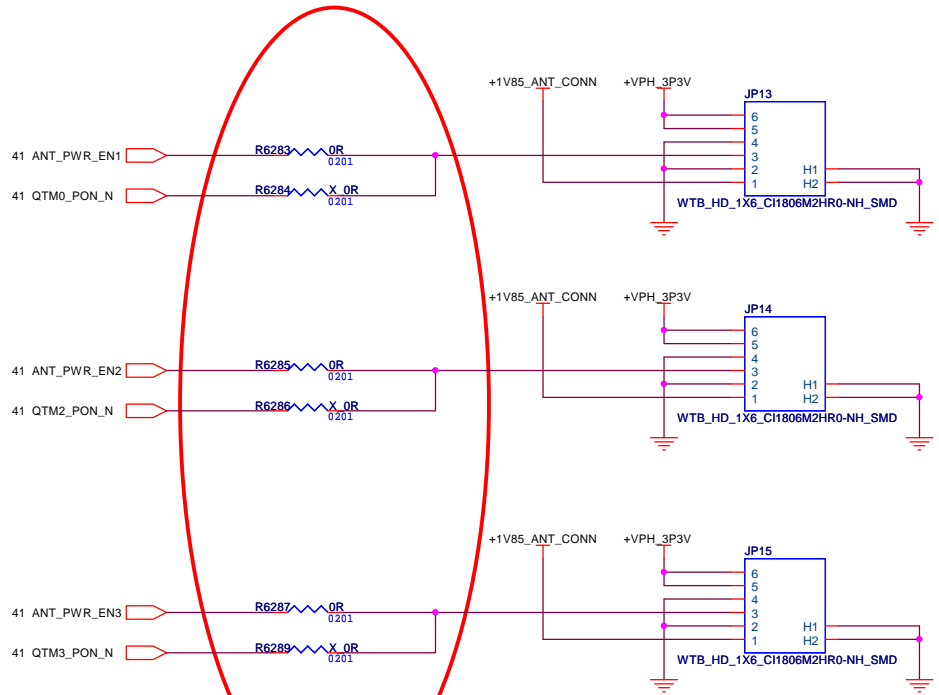





UIM & ANT PWR CONN
RESERVED



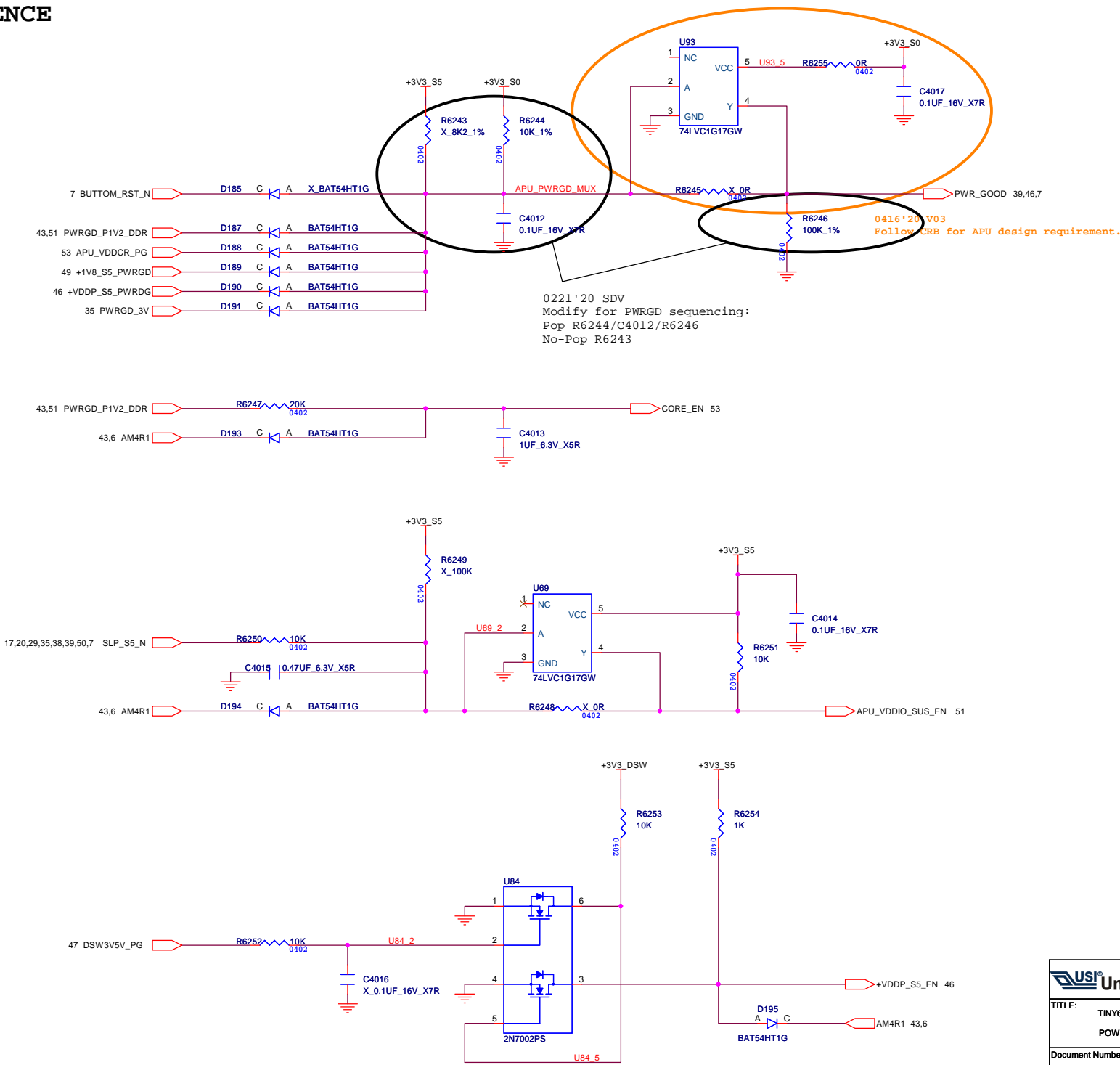
0414'20 V03
Co-lay mmWave PWR_EN pin
for 5G 3052 card



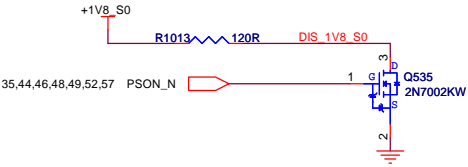
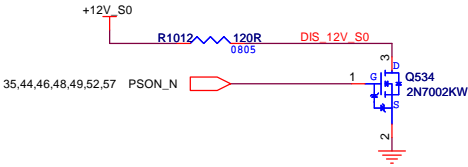
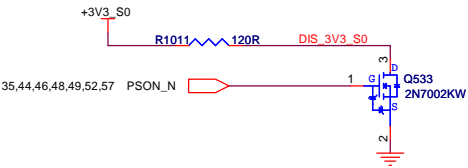
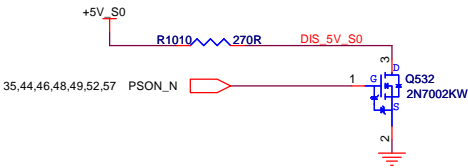
0414'20 V03
Co-lay mmWave PWR_EN pin
for 5G 3052 card

 Universal Scientific Industrial Co., Ltd.			
TITLE:		REV:	
TINY6 M75Q-2		V0.3	
UIM & ANT PWR CONN			
Document Number : <Doc>			
Prepared by : <i>Jason</i>			
SIZE :	A3	Date:	Tuesday, April 28, 2020
PAGE:	42 of 66		

POWER SEQUENCE

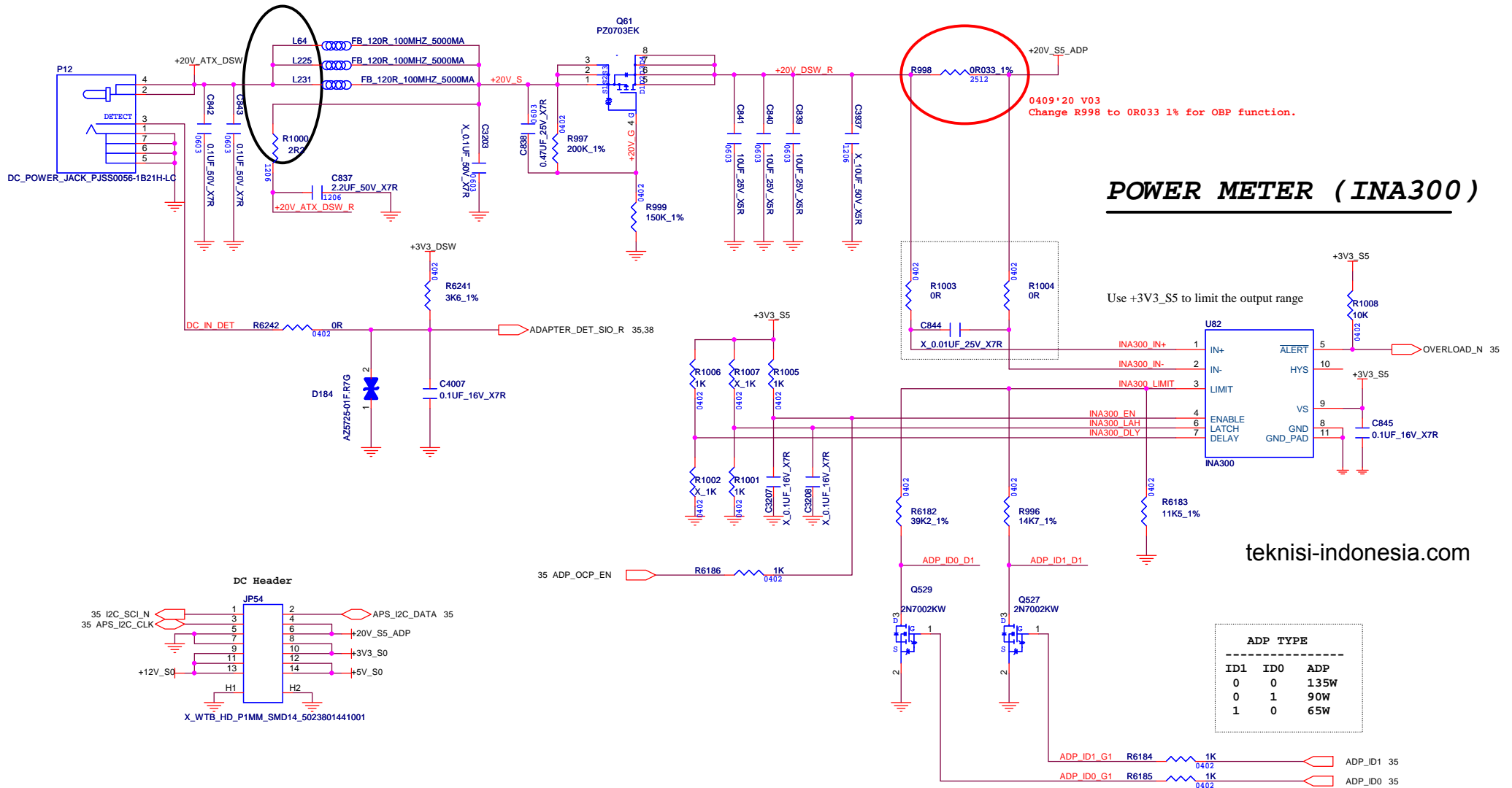


POWER DISCHARGE



DC IN 20V

```
0221'20 SDV
Correct the connection of R1000
```



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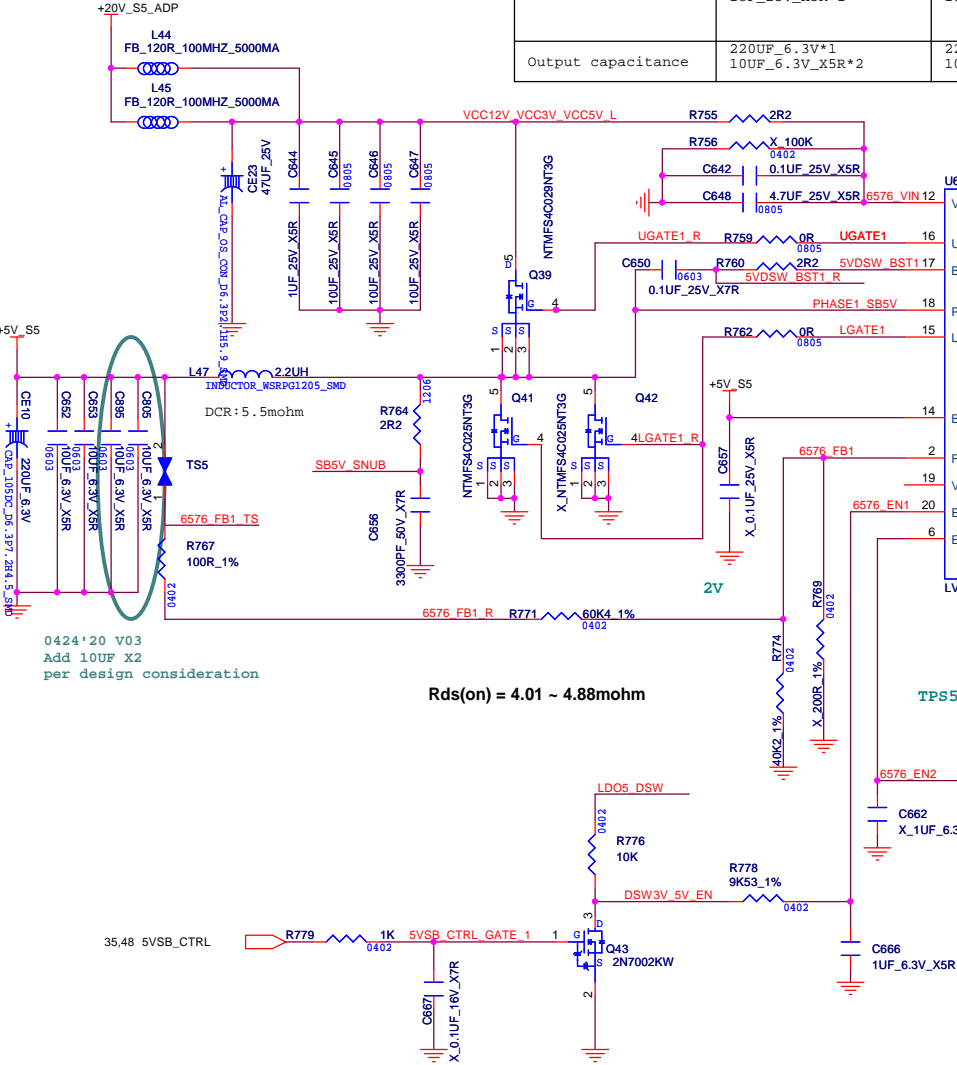
ADP TYPE		
ID1	ID0	ADP
0	0	135W
0	1	90W
1	0	65W

Enable	Disable
EN1,EN2 > 1.4 V	EN1,EN2 < 0.4 V

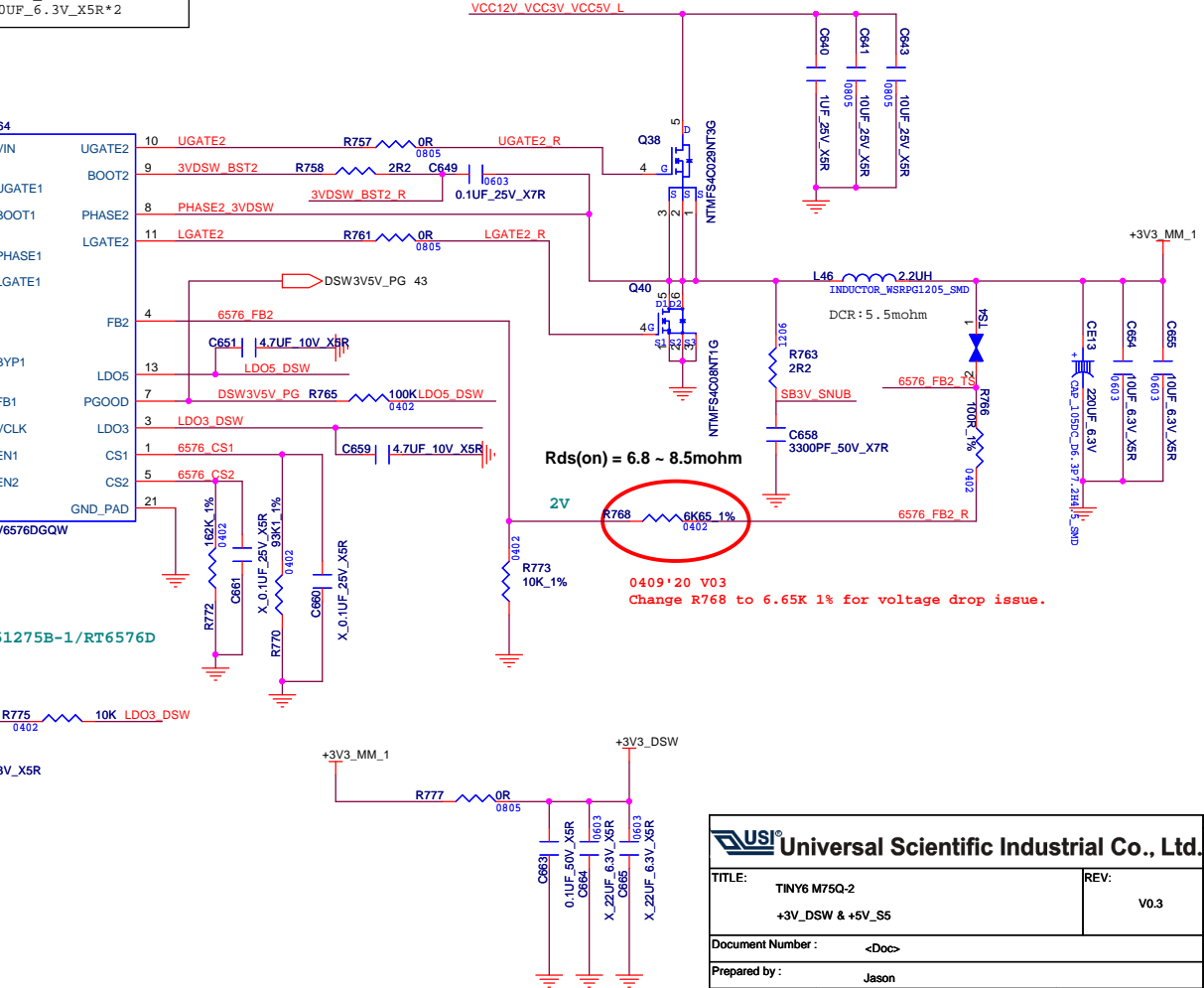
Parameter	+5V_S5	+3V_MM_1
Iout.max	14A	17A
OCp set point	23A	25.8A
OCp formula	RLIMIT=(ILIMITxRDS(ON))x8/10µA	RLIMIT=(ILIMITxRDS(ON))x8/10µA
Switching Frequency	300kHz	355kHz
Input ripple current	6.063A	6.31A
Choke_size(L*W*H) (mm)	13.8*12.9*5	13.8*12.9*5
Choke_Isat	32A	32A
Choke_DCR	5.5mΩ	5.5mΩ
Choke_LIR	40.6%	20.8%
Input capacitance	10UF_25V_X5R*3 1UF_25V_X5R*1	10UF_25V_X5R*2 1UF_25V_X5R*1
Output capacitance	220UF_6.3V*1 10UF_6.3V_X5R*2	220UF_6.3V*1 10UF_6.3V_X5R*2


+5V_S5/+3V3_MM_1

+5V_S5
Max. output=14A
OCp:23A



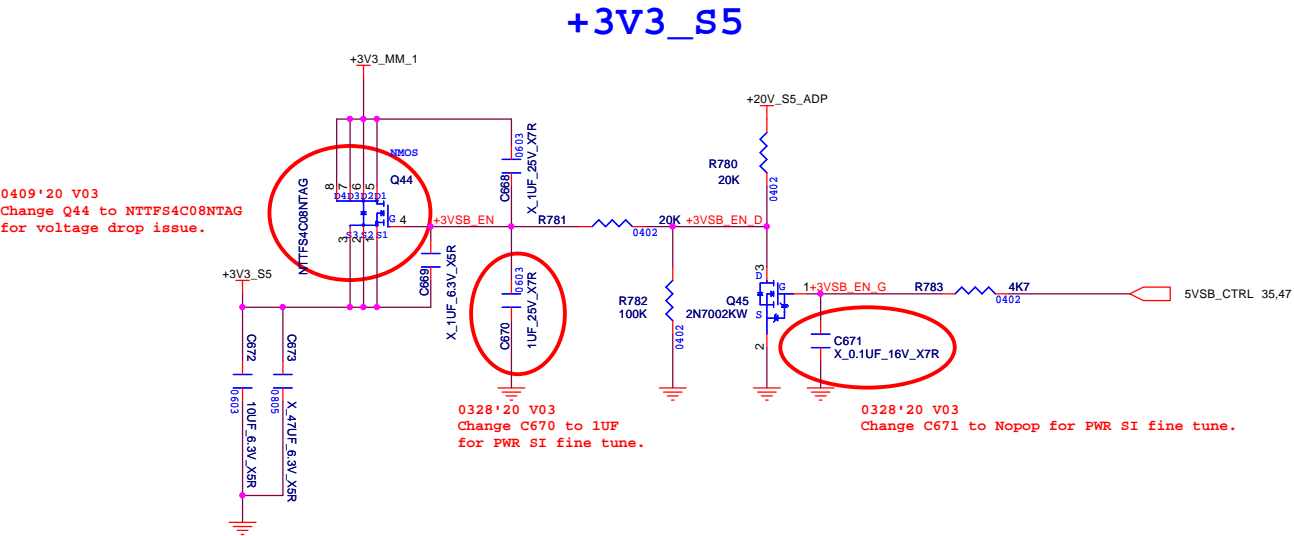
+3V_MM_1
Max. output=10A
OCp:18A



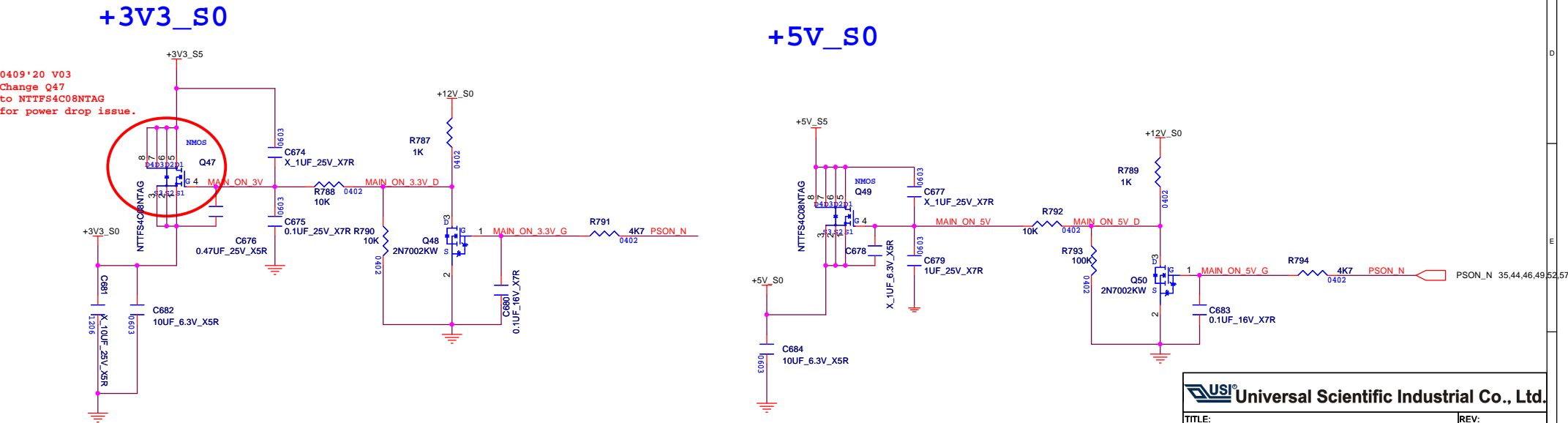

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TITLE: TINY6 M75Q-2 +3V_DS_W & +5V_S5		REV: V0.3
Document Number : <Doc>		
Prepared by : Jason		
SIZE : A3	Date: Tuesday, April 28, 2020	PAGE: 47 of 66

STAND BY POWER CONTROL

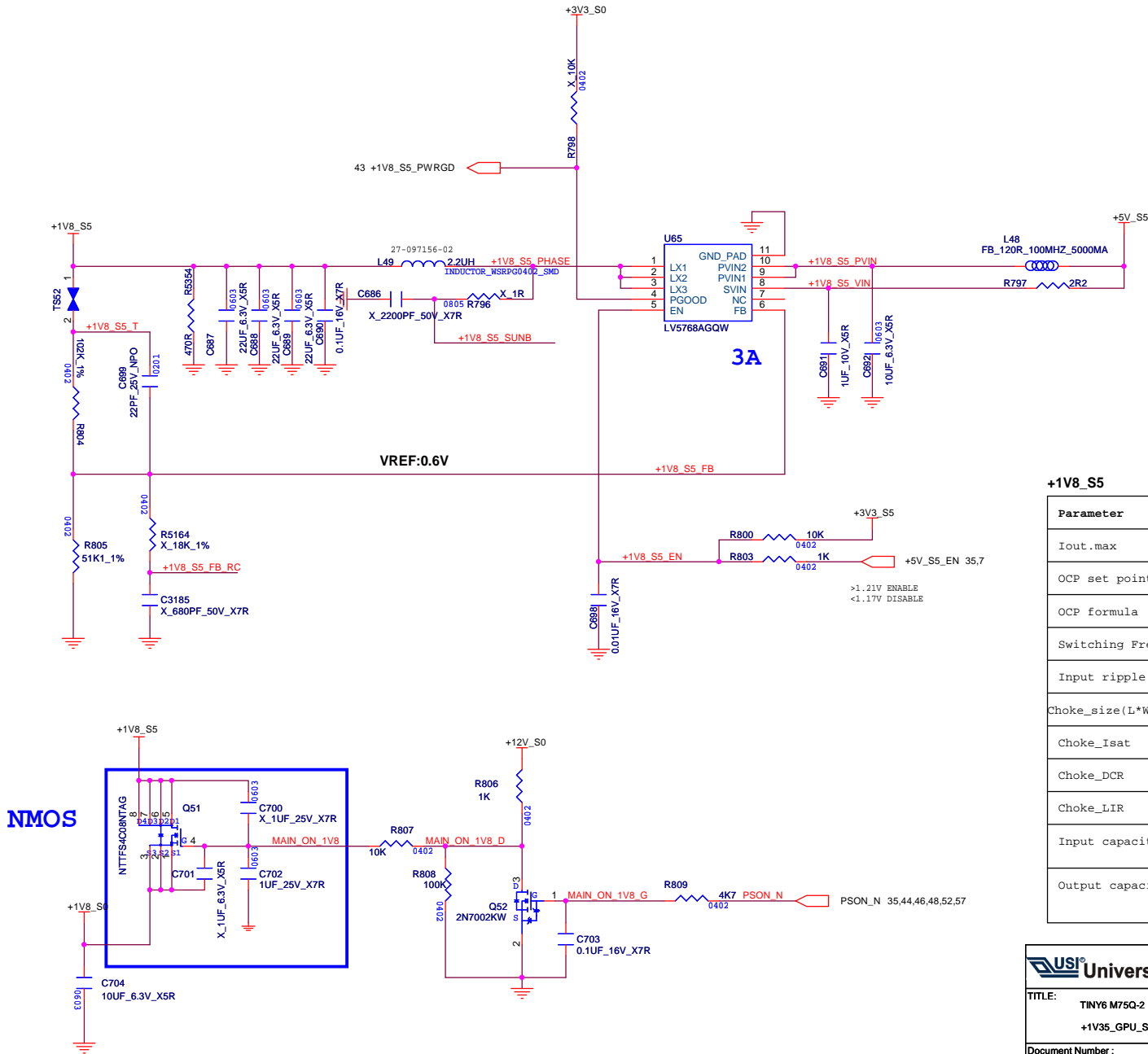


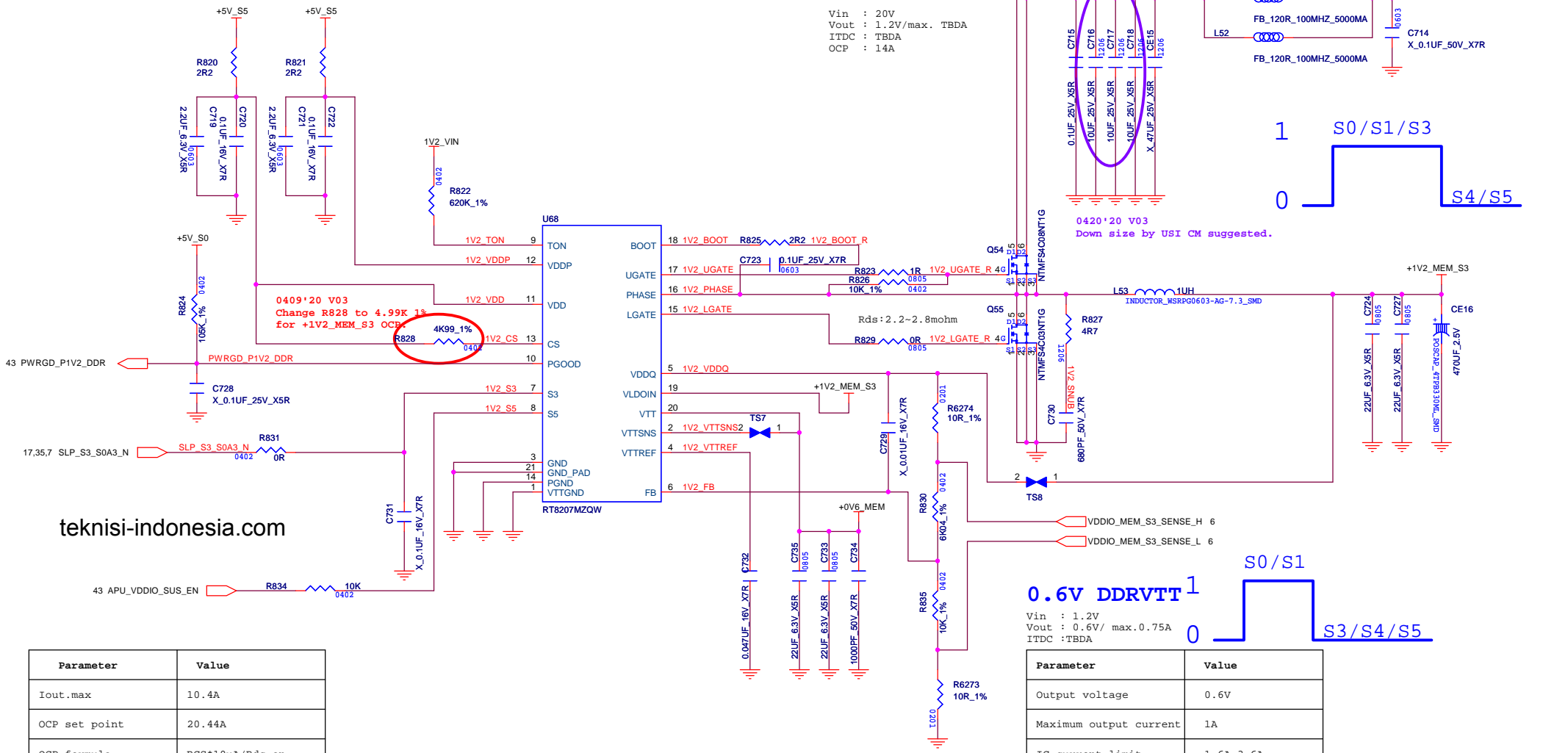
SYSTEM POWER CONTROL



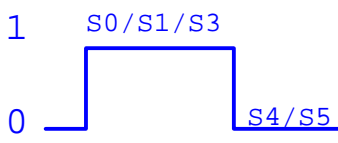
+1V8_S5

TDC: 2.25A





DDR4 1.2V
Vin : 20V
Vout : 1.2V/max. TBDA
ITDC : TBDA
OCP : 14A



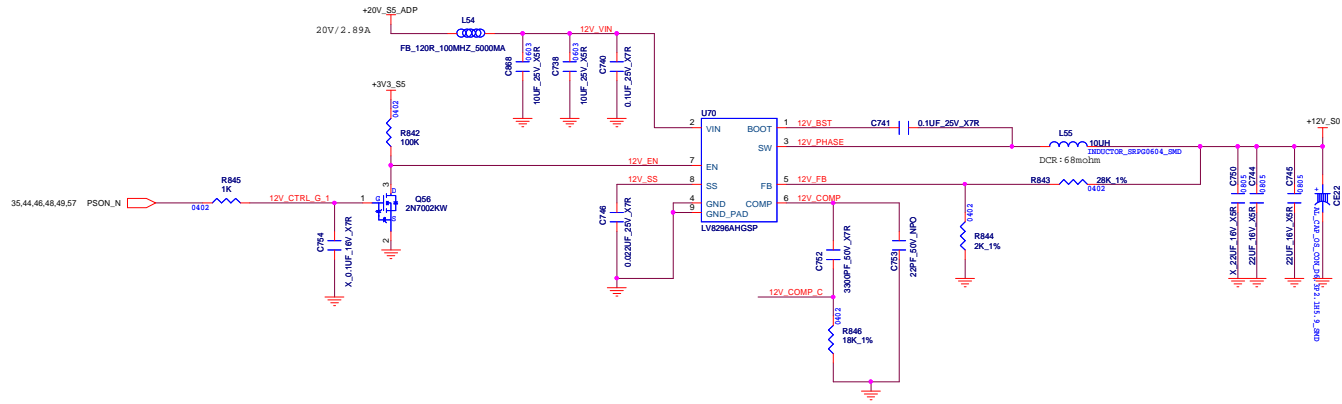
0.6V DDRVTT
Vin : 1.2V
Vout : 0.6V/ max.0.75A
ITDC :TBDA

Parameter	Value
Output voltage	0.6V
Maximum output current	1A
IC current limit	1.6A-3.6A
Max. PD(theoretically)	0.6W
Rja	68°C/W
Enable condition	" +3V_S5" ON

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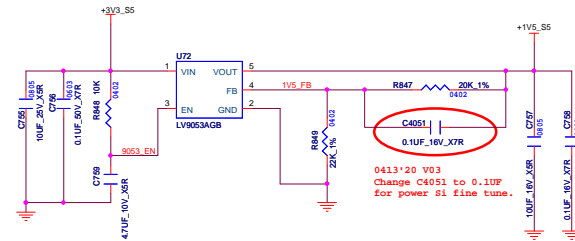
Parameter	Value
Iout.max	10.4A
OCP set point	20.44A
OCP formula	RCS*10uA/Rds_on
Switching Frequency	408kHz
Input ripple current	2.47A
Choke_size(L*W*H)(mm)	7.6*6.8*3
Choke_Isat	22A
Choke_DCR	10mΩ
Choke_LIR	26.6%
Input capacitance	10UF_25V_X5R*3 0.1UF_25V_X5R*1
Output capacitance	470UF_2.5V*1 22UF_6.3V_X5R*2

USI® Universal Scientific Industrial Co., Ltd.		
TITLE: TINY6 M75Q-2 System DDR4 VR		REV: V0.3
Document Number : <Doc>		
Prepared by : Jason		
SIZE : A3	Date: Tuesday, April 28, 2020	PAGE: 51 of 66



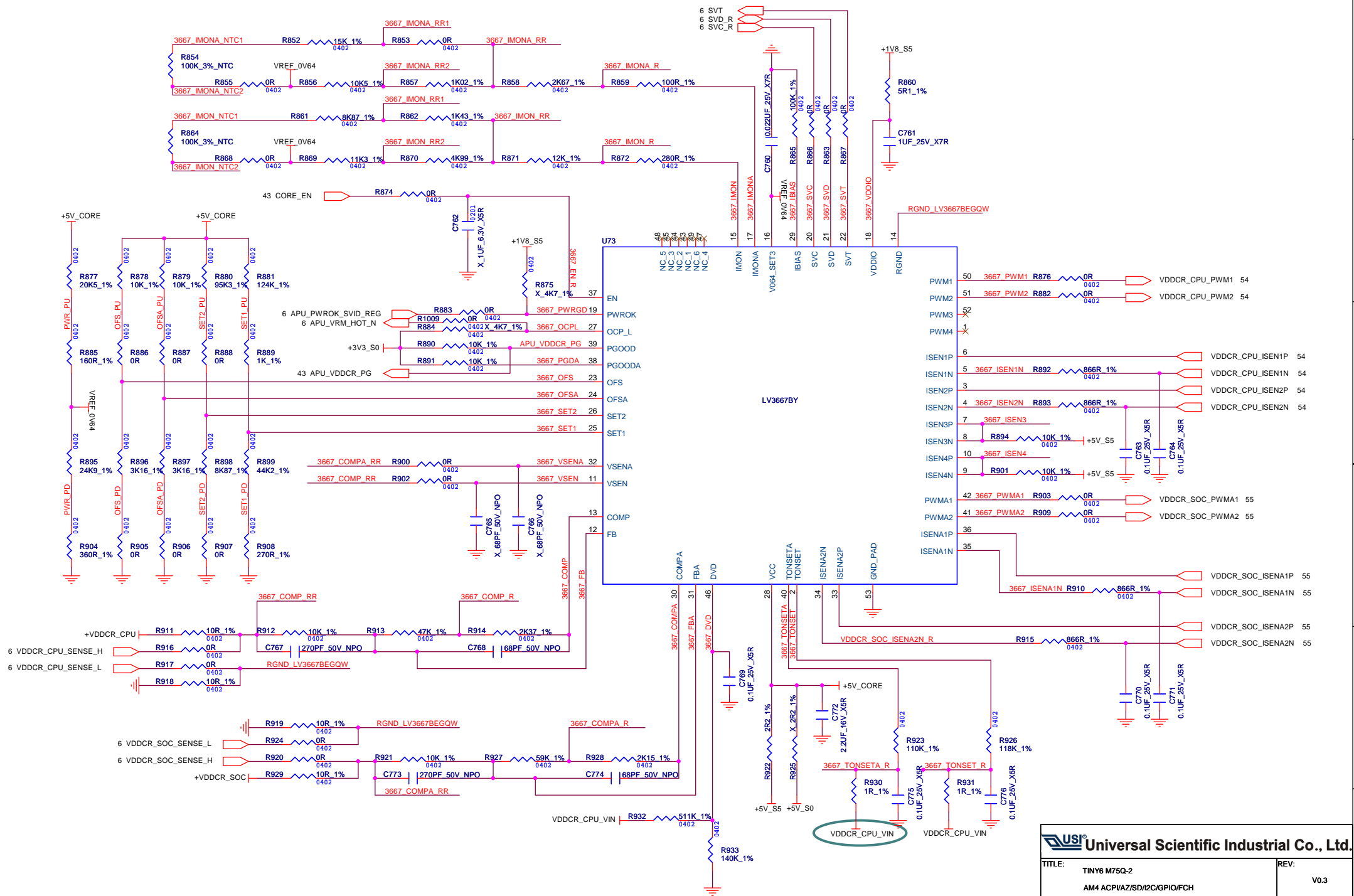
+12V_S0

Parameter	Value
Iout.max	2.201A
OCF set point	3.8A-6.4A
OCF formula	IC Controlled
Switching Frequency	340kHz
Input ripple current	1.13A
Choke_size(L*W*H)(mm)	11.5*10.3*4.0
Choke_Isat	8.5A
Choke_DCR	30mΩ
Choke_LIR	64.1%
Input capacitance	100µF_25V_X5R*2 0.1µF_25V_X7R*1
Output capacitance	22µF_16V_X5R*2 47µF_25V*1



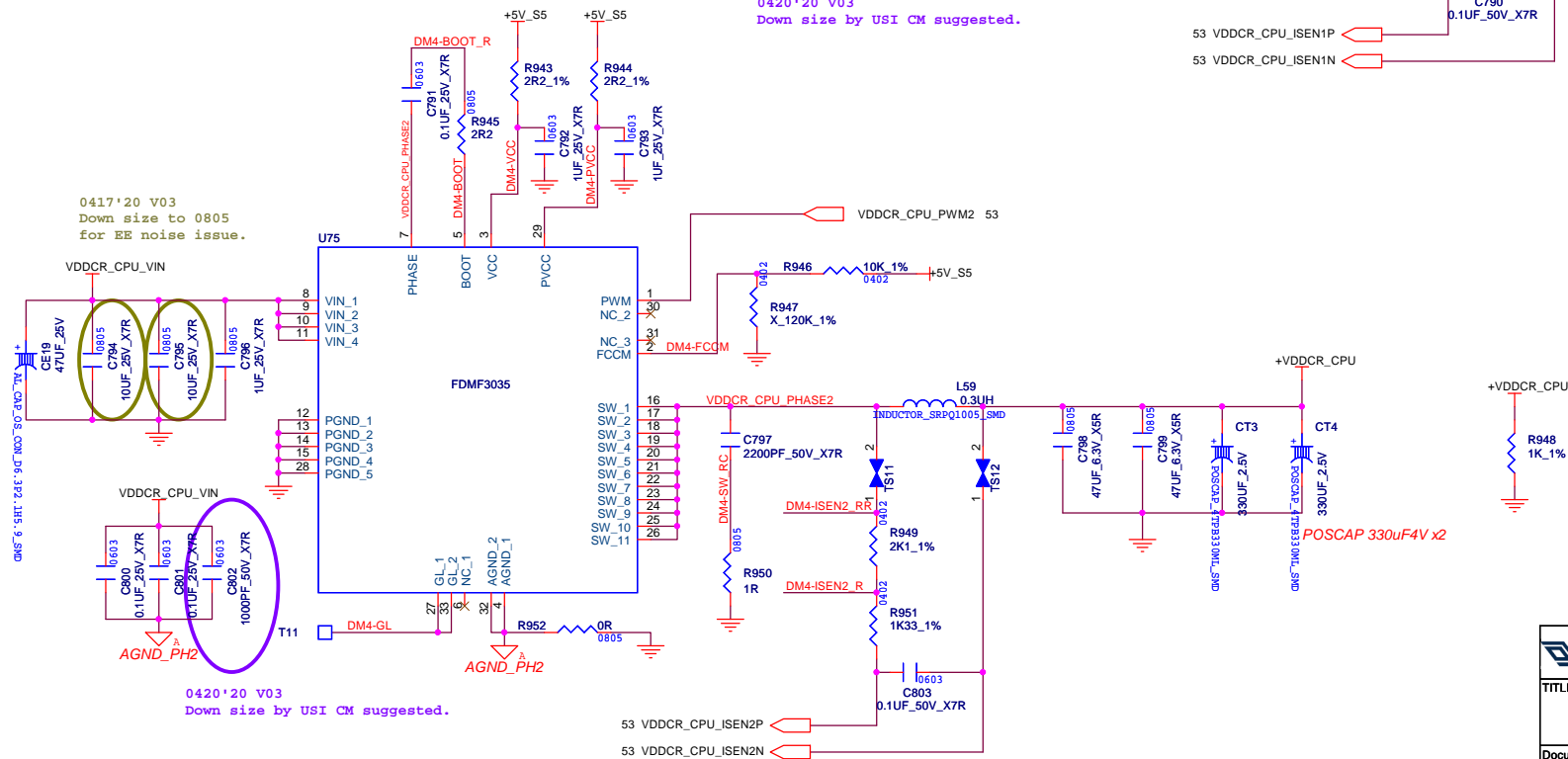
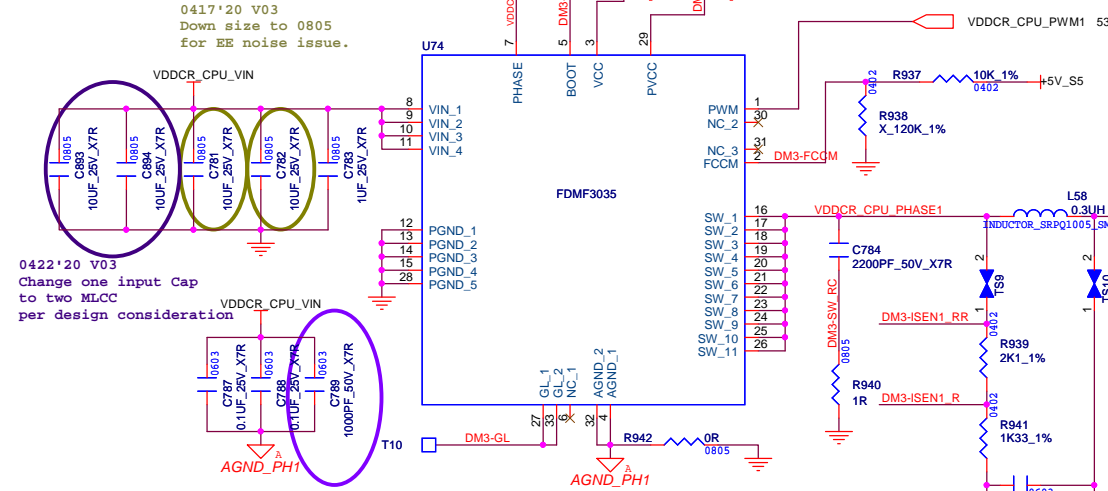
+1V5_S5

Parameter	Value
Iout.max	0.276A
OCF set point	0.4A-1A
OCF formula	IC controlled
Input ripple current	0.138A
Input capacitance	100µF_25V_X5R*1 0.1µF_50V_X7R*1
Output capacitance	100µF_16V_X5R*1 0.1µF_16V_X7R*1



VDDCR_CPU

Parameter	Value
Iout.max	55A
OCP set point	70A
OCP formula	$IL_SUM(SPIKE) = (3.19375 - 0.64/DCRL) \times (Rcsx/RIMON)$
Switching Frequency	359kHz
Input ripple current	8.604A
Choke_size(L*W*H) (mm)	11X7.2X5
Choke_Isat	61A
Choke_DCR	1.05mΩ
Choke_LIR	35.1%
Input capacitance	10UF_25V_X7R*4 1UF_25V_X7R*2 47UF_25V*2
Output capacitance	330UF_4V*4 47UF_6.3V_X5R*4



0424'20 V03
Remove L60,L61 for interleave
per design consideration

0424'20 V03
For interleave
per design consideration

0417'20 V03
Down size to 0805
for EE noise issue.

VDDCR_SOC

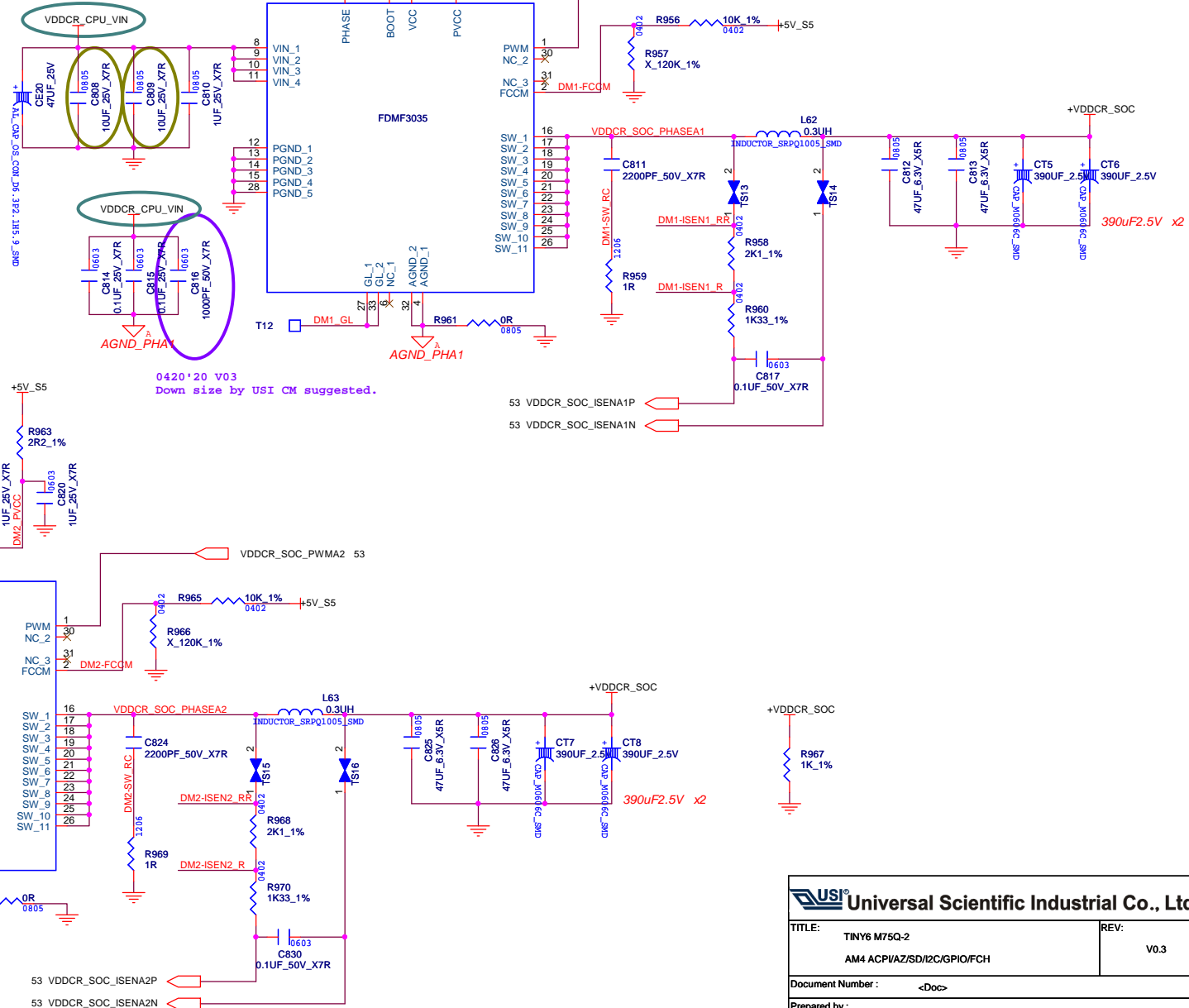
Parameter	Value
Iout.max	60A
OCP set point	70A
OCP formula	$IL_SUM(SPIKE) = (3.19375 - 0.64/DCRL) \times (Rcsx/RIMON)$
Switching Frequency	375kHz
Input ripple current	9.387A
Choke_size(L*W*H)(mm)	11X7.2X5
Choke_Isat	61A
Choke_DCR	1.05mΩ
Choke_LIR	30.8%
Input capacitance	10UF_25V_X7R*4 1UF_25V_X7R*2 47UF_25V*2
Output capacitance	390UF_2.5V*4 47UF_6.3V_X5R*4

0424'20 V03
For interleave
per design consideration

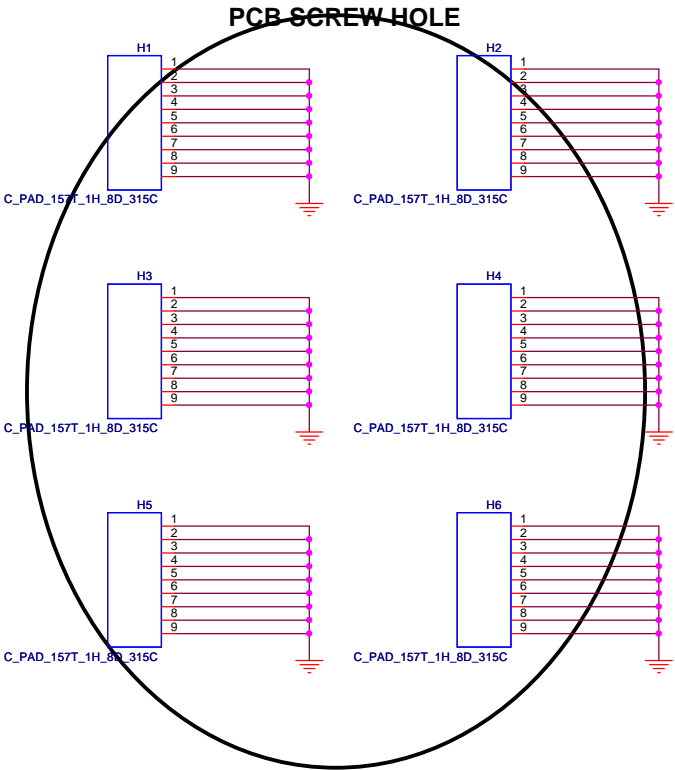
0422'20 V03
Change one input Cap
to two MLCC
per design consideration

0417'20 V03
Down size to 0805
for EE noise issue

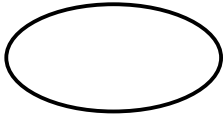
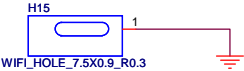
0420'20 V03
Down size by USI CM suggested.



SCREW HOLE



0221'20 SDV
Change to PTH hole



0221'20 SDV
Del holes

M.2 WIFI STAND OFF HOLE



BTB STAND OFF HOLE



SSD CARD STAND OFF HOLE



SINGAL PORT LAN CARD STAND OFF HOLE



APU SCREW HOLE




M.2 5G STAND OFF HOLE

SCREW_H_295T174B_D154PS_H102

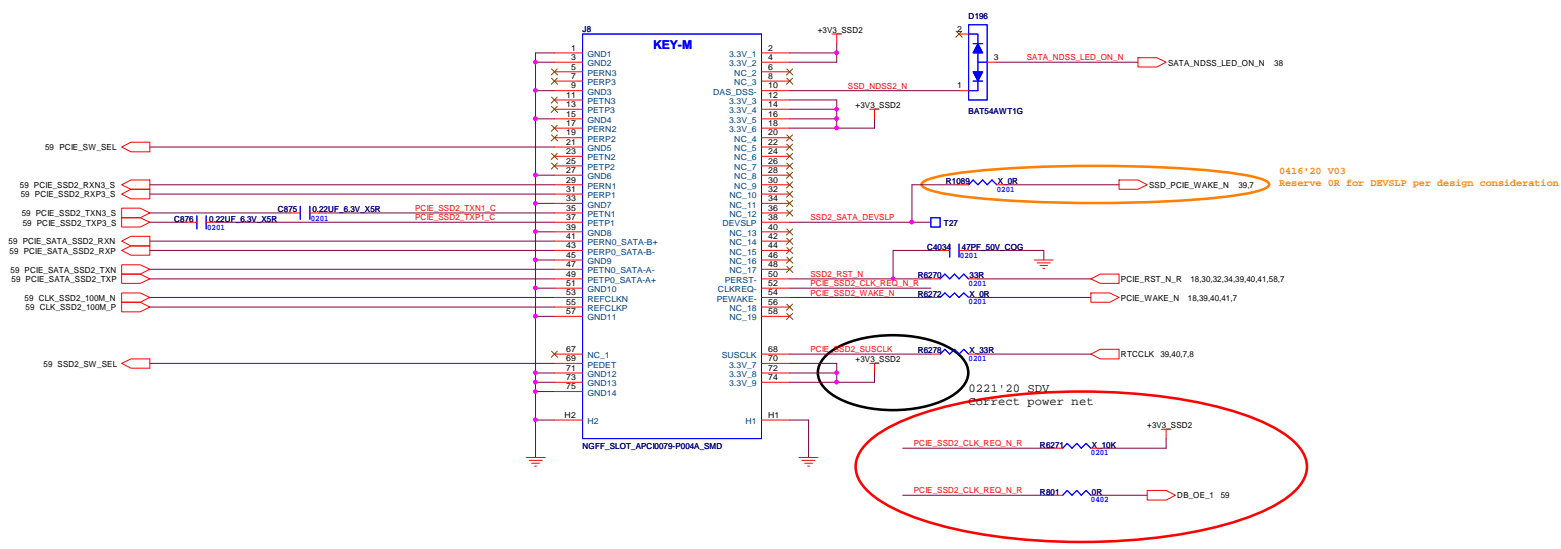


0417'20 V03
Change 5G standoff hole for DXF updated.

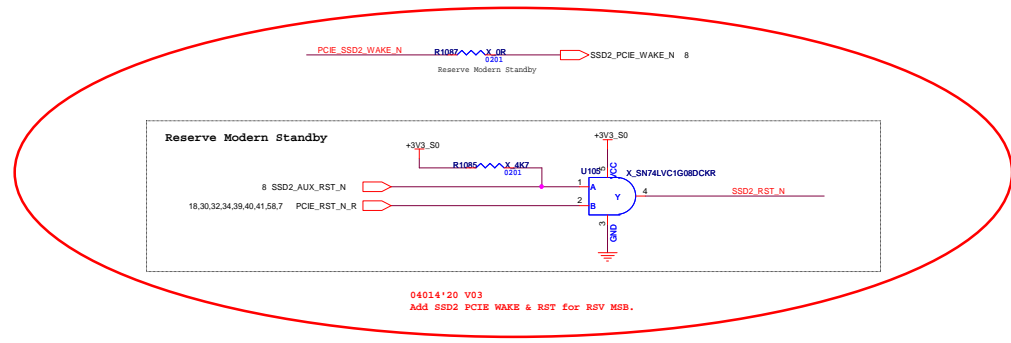
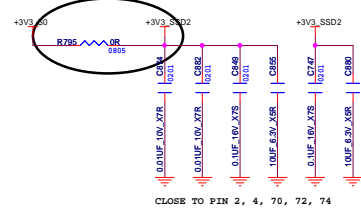
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TITLE: TINY6 M75Q-2 SCREW HOLE			REV: V0.3
Document Number : <Doc>			
Prepared by : <i>Jason</i>			
SIZE : A3	Date: Tuesday, April 28, 2020	PAGE:	56 of 66

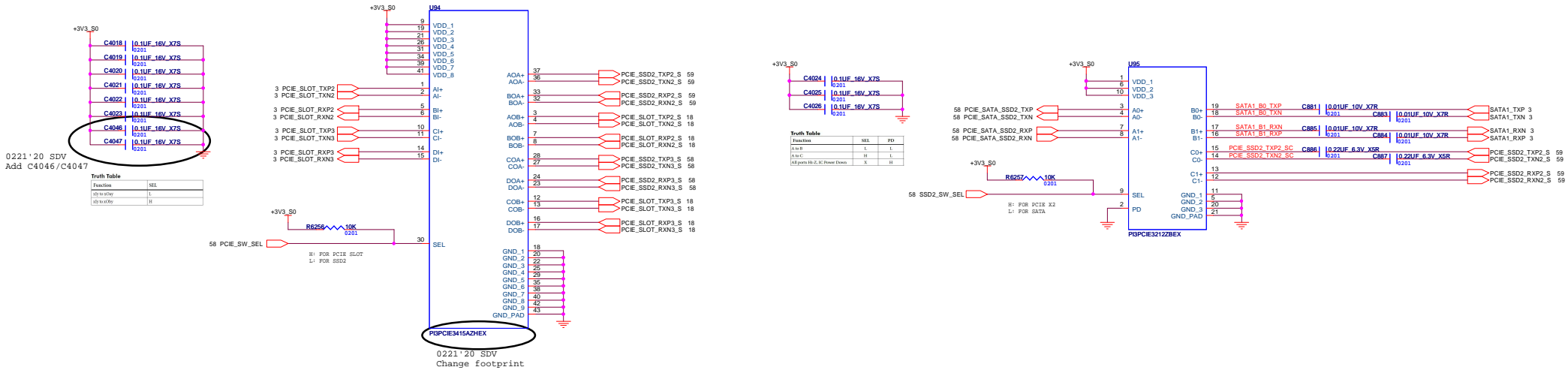
[illegible]



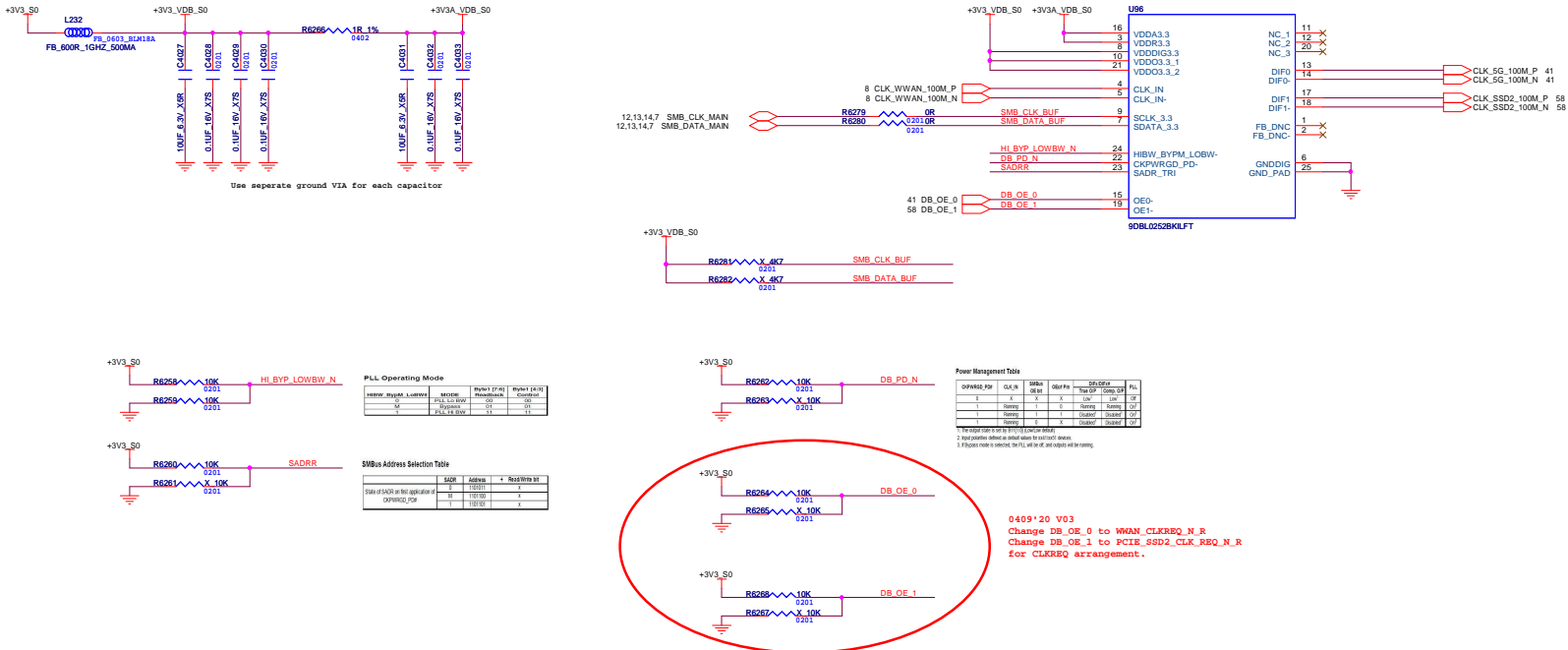
0221*20 SDV
Change footprint from 0402 to 0805



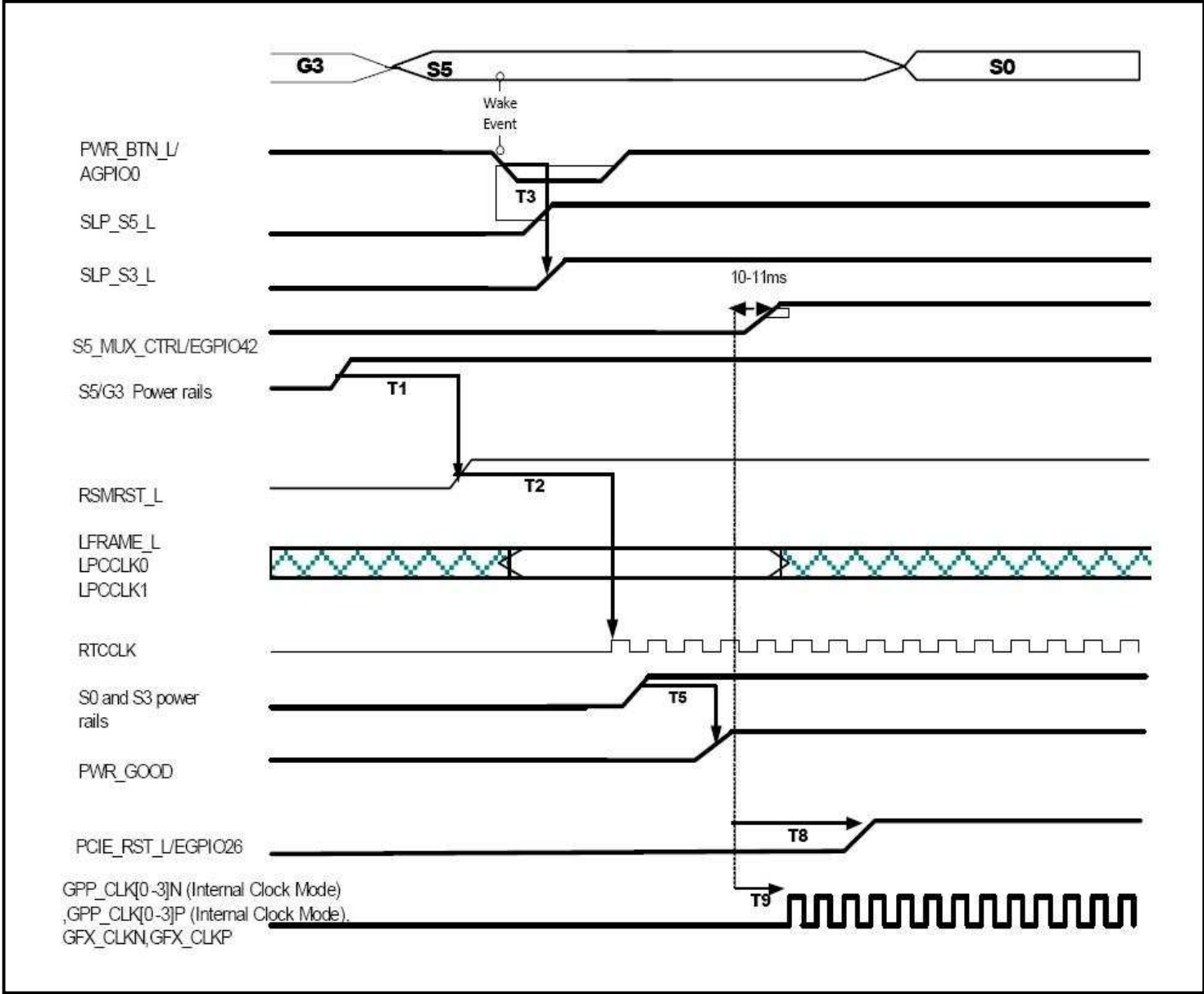
PCIE SWITCH



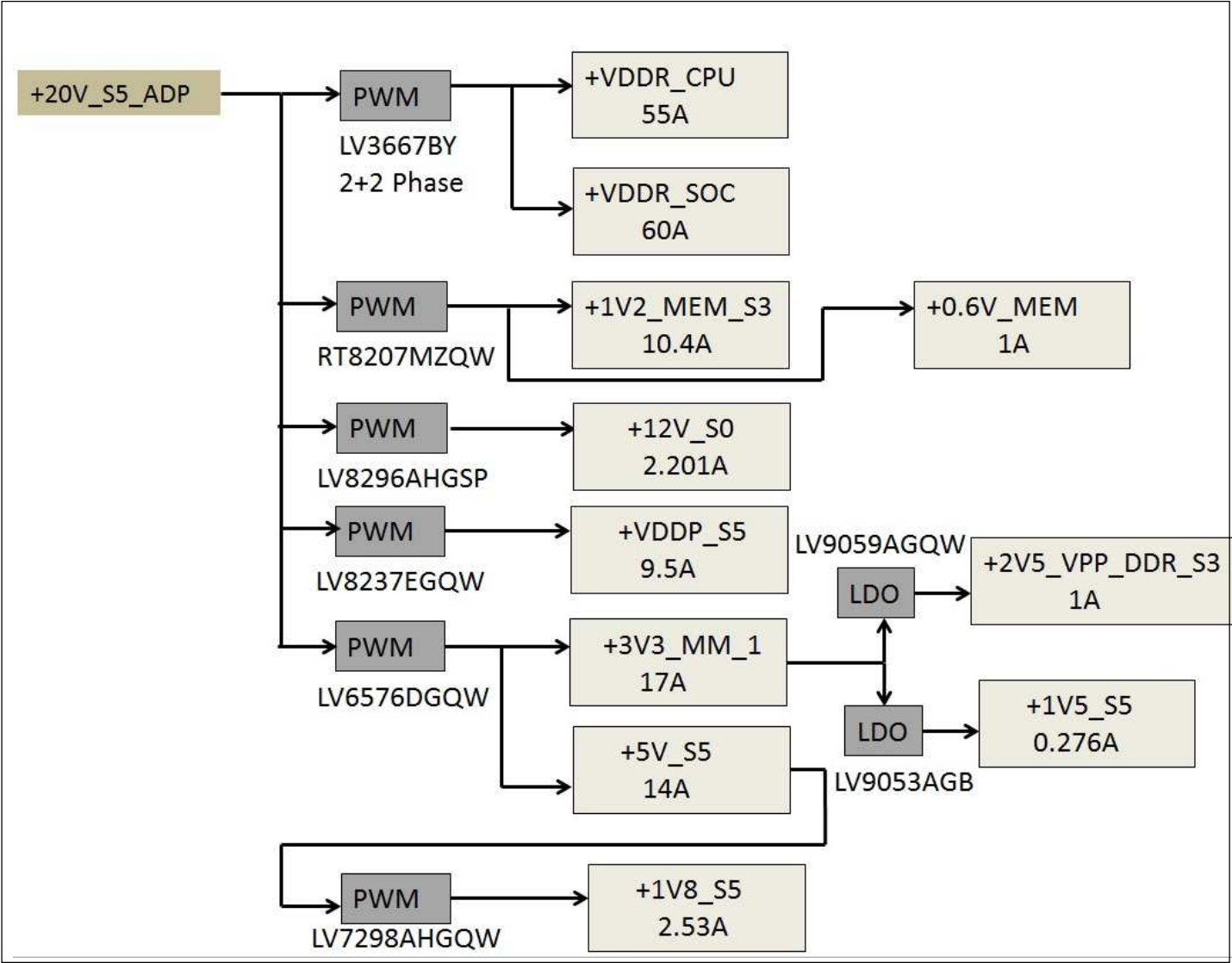
CLOCK BUFFER



PWR SEQUENCE DIAGRAM



PWR DELIVERY DIAGRAM

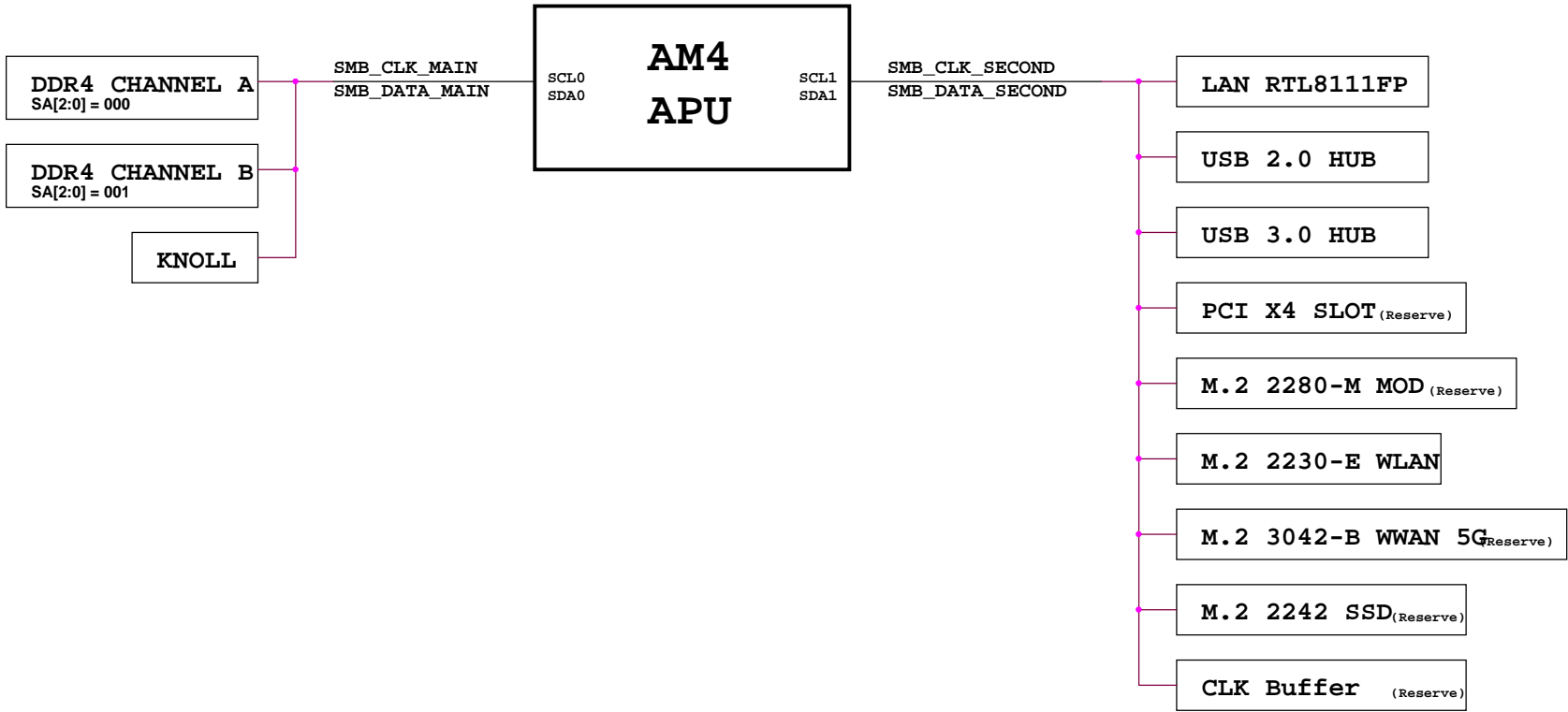


GPIO TABLE

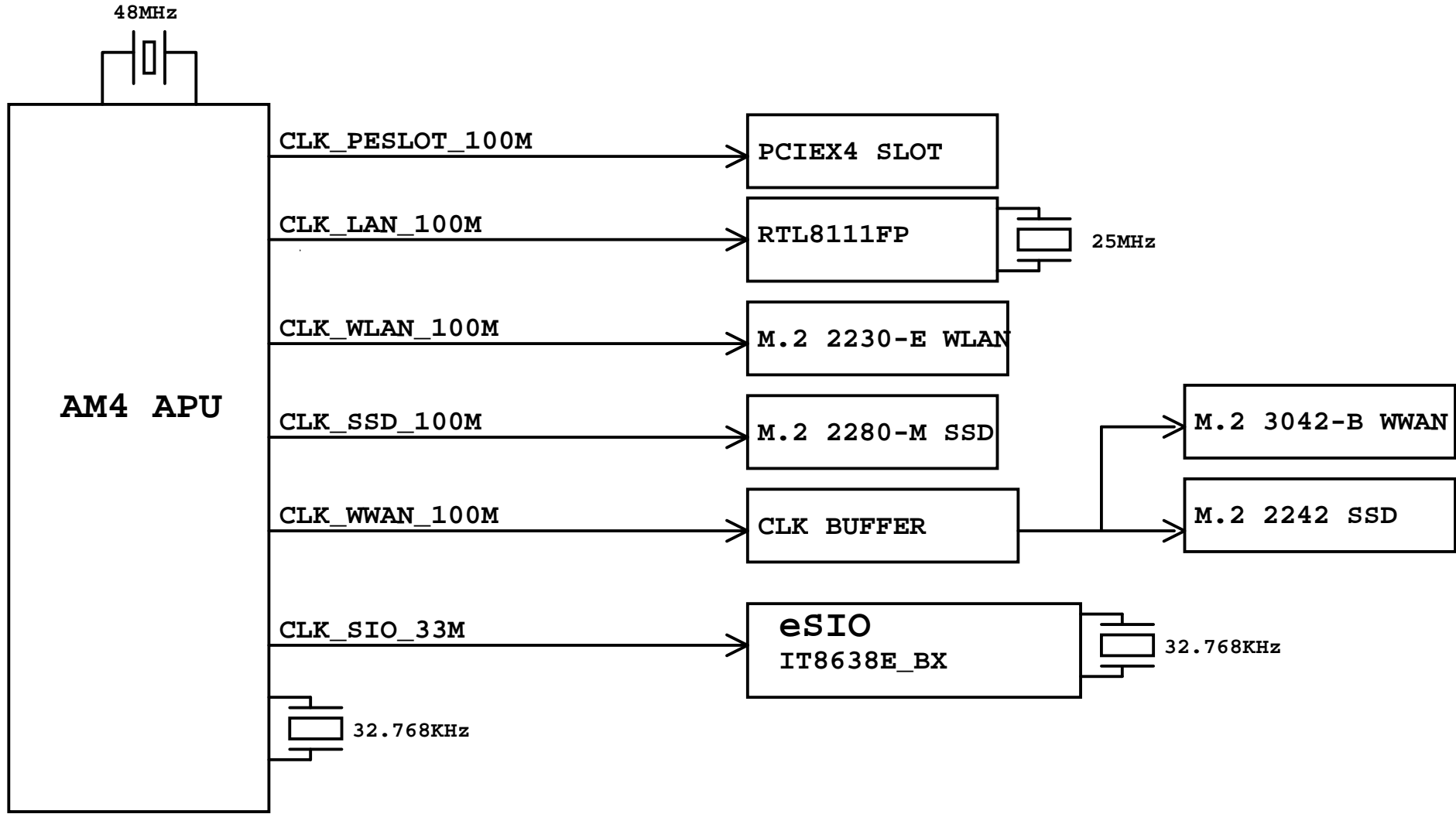
PIN No.	SIO Pin Name	Tiny 6 AMD Usage	Power Domain	Default H/L
1	5VSB_CTRL_CIRR2_GP16	Reserve for 5VSB_CTRL	3VSB(+3V3_DSW_SIO)	L
2	PCIRSTIN_CIRT2_GP15_CPU_PG	PU to 3VSB	3VSB(+3V3_DSW_SIO)	H
4	VCORE_EN_PCH_C1_GP14	NC		H
5	SLP_SUS_VLDT_EN_GP63	NC		H
7	FAN_TAC1	FAN_TACH	3VSB(+3V3_DSW_SIO)	H
8	FAN_CTL1	FAN_PWM	3VSB(+3V3_DSW_SIO)	H
9	FAN_TAC2_GP52	5VSB_CTRL	3VSB(+3V3_DSW_SIO)	H
10	FAN_CTL2_GP51	GBE_EN_N	3VSB(+3V3_DSW_SIO)	H
11	FAN_TAC3_GP37	BTB_DP0_DET_N	3VSB(+3V3_DSW_SIO)	H
12	FAN_CTL3_GP36	COM_A_DET_N	3VSB(+3V3_DSW_SIO)	H
13	F_DIO3_GP35	NC		H
14	DPWR0K_GP32	PWRBTN_LED	3VSB(+3V3_DSW_SIO)	H
16	F_DIO2_GP30	NC		H
17	SIN2_GP27	SIN2_N	VCC3(+3V3_S0)	H
18	SOUT2_GP26	SOUT2_N	VCC3(+3V3_S0)	H
19	DSR2_GP25	DSR2_N	VCC3(+3V3_S0)	H
20	RTS2_GP24	RTS2_N	VCC3(+3V3_S0)	H
21	SI_GP23	SIO_SI	VFSPI(+3V3_DSW_SIO)	H
22	SCK_GP22	SIO_SCK	VFSPI(+3V3_DSW_SIO)	H
23	DCD2_GP21	DCD2_N	VCC3(+3V3_S0)	H
24	CTS2_GP20	CTS2_N	VCC3(+3V3_S0)	H
25	RI2_GP17	RI2_N	3VSB(+3V3_DSW_SIO)	H
26	DTR2_GPA7	DTR2_N	VCC3(+3V3_S0)	H
27	CE_N_CIRTX1	SIO_CS_N	VFSPI(+3V3_DSW_SIO)	H
28	GP50	SIO_S0	VFSPI(+3V3_DSW_SIO)	L
29	PWR0K1_GP13	PWRGD_3V	VCC3(+3V3_S0)	L
30	PCIRST1_PCH_D1_GP12	SIO_AZ_MUTE_N	3VSB(+3V3_DSW_SIO)	L
31	PCIRST2_GP11	HUB2_RESET_N	3VSB(+3V3_DSW_SIO)	L
36	ESPI_ALERT_SERIRQ	LPC_SERIRQ	VCCBT(+3V3_S5)	H
37	ESPI_CS_LFRAME-	LPC_FRAME_N	VCCBT(+3V3_S5)	H
38	ESPI0_LAD0	LPC_AD0	VCCBT(+3V3_S5)	H
39	ESPI0_LAD1	LPC_AD1	VCCBT(+3V3_S5)	H
40	ESPI0_LAD2	LPC_AD2	VCCBT(+3V3_S5)	H
41	ESPI0_LAD3	LPC_AD3	VCCBT(+3V3_S5)	H
42	CLKIN_E_KRST-	KBRST_N	VCC3(+3V3_S0)	H
43	ESPI_RESET_GA20_GP82	NC		H
44	ESPI_CLK_PICLK	CLK_SIO_33M	VCCBT(+3V3_S5)	H
45	LDRQ_GP92	LPC_DRQ0_N	VCCBT(+3V3_S5)	H
46	PLTRST_LRESET-	APU_PLT_RST_N_SIO	VCCBT(+3V3_S5)	H
48	SMBCLK1_GP65	SIO_SMBCLK1	3VSB(+3V3_DSW_SIO)	H
49	SMBDAT1_GP66	SIO_SMBDAT1	3VSB(+3V3_DSW_SIO)	H
50	SST_AMDTSI_D_GP62	AMDTSI_D	VCC3(+3V3_S0)	H
51	PECI_AMDTSI_C_GP64	AMDTSI_C	VCC3(+3V3_S0)	H
52	PWMOUT0_GP31	I2C_SCI_N	3VSB(+3V3_DSW_SIO)	H
53	PWMOUT1_GPA0	NC		H
54	USBSW1_DM	RUSB3_USB2N	3VSB(+3V3_DSW_SIO)	H
55	USBSW1_DP	RUSB3_USB2P	3VSB(+3V3_DSW_SIO)	H
56	USBSW1_YM	USBSW1_SIO_YM	3VSB(+3V3_DSW_SIO)	H
57	USBSW1_YP	USBSW1_SIO_YP	3VSB(+3V3_DSW_SIO)	H
58	GP86_SMBCLK0	AP5_I2C_CLK	3VSB(+3V3_DSW_SIO)	H
59	IO_SCI_GP85_SMBDAT0	AP5_I2C_DATA	3VSB(+3V3_DSW_SIO)	H
60	SMBDAT2_GP47	WWAN_PWR_EN		H
61	SMBCLK2_GP46	WWAN_PWR_EN		H
65	COPEN-	INTRD_IN_N	+3V_BATT	H
68	SUSB_GP45	SLP_S3_S0A3_N	3VSB(+3V3_DSW_SIO)	H
69	PWR0N_GP44	PWRBTN_OUT_SIO_N	3VSB(+3V3_DSW_SIO)	H
70	ME_GP54_USBPWREN1-	OBP_PROCHOT	3VSB(+3V3_DSW_SIO)	H
72	PANSWH_GP43	PWRBTN_N	3VSB(+3V3_DSW_SIO)	H
73	PSON_GP42	PSON_N	3VSB(+3V3_DSW_SIO)	H
74	SUSC_GP53	SLP_S5_N	3VSB(+3V3_DSW_SIO)	H
75	PWR0K2_GP41_S0A	PU to VCC3	VCC3(+3V3_S0)	L
76	3VSB5W_GP40_SCL	SIO_DELAYPCIERST_N	VCC3(+3V3_S0)	H
77	KDAT_GP61	WWAN_PE_RESET_N	3VSB(+3V3_DSW_SIO)	H
78	KCLK_GP60	M2_PDET_N	3VSB(+3V3_DSW_SIO)	H
79	MDAT_GP57	BTB_USB_DET_N	3VSB(+3V3_DSW_SIO)	H
80	MCLK_GP56	HUB3_SMB_CTL	3VSB(+3V3_DSW_SIO)	H
81	PCIRST3_GP10	LAN_WAKE_N	3VSB(+3V3_DSW_SIO)	L
82	RSMRST_CIRR1_GP55	RSMRST_SIO_N	3VSB(+3V3_DSW_SIO)	H
84	TS0	THERMDC	A3VSB(+3V3_DSW_SIO)	H
85	TMPIN3	SYS_THERMDA	A3VSB(+3V3_DSW_SIO)	H
86	TMPIN2	M2_THERMDA	A3VSB(+3V3_DSW_SIO)	H
87	TMPIN1	VRM_THERMDA	A3VSB(+3V3_DSW_SIO)	H
97	GP93	HUB_SMB_CTL	3VSB(+3V3_DSW_SIO)	H
98	ATXPG_GP94	PWRGD_P5U_SIO	VCC3(+3V3_S0)	H
99	FAN_TAC4_GP95	KERNEL_DBG_N	3VSB(+3V3_DSW_SIO)	H
100	GP96_CLKRUN-	SSD_PWR_EN	3VSB(+3V3_DSW_SIO)	H
101	SLCT_GP97	PM_WWAN_DISABLE_N	3VSB(+3V3_DSW_SIO)	H
102	PE_GP80	SIO_SCI	3VSB(+3V3_DSW_SIO)	H
103	BUSY_GP81	OVERLOAD_N_R	3VSB(+3V3_DSW_SIO)	H
104	GPACK_GP82	WWAN_BT_DET_N	3VSB(+3V3_DSW_SIO)	L
105	SUP_GP83	ADP_ID1	3VSB(+3V3_DSW_SIO)	H
106	INIT_GP84	ADP_ID0	3VSB(+3V3_DSW_SIO)	H
107	ERR_GP87	ADP_OCP_EN	3VSB(+3V3_DSW_SIO)	H
108	AFD_GP90	2543_P2_EN_R	3VSB(+3V3_DSW_SIO)	H
109	STB_GP91	2543_CTL3_R	VCC3(+3V3_S0)	H
110	KSIO_PD0_GP70	2543_CTL2_R	3VSB(+3V3_DSW_SIO)	H
111	KS14_PDL1_GP71	2543_CTL1_R	3VSB(+3V3_DSW_SIO)	H
112	KS00_PD2_GP72	WWAN_DET_N	3VSB(+3V3_DSW_SIO)	H
113	KS01_PD3_GP73	BOARDID0	3VSB(+3V3_DSW_SIO)	H
114	KS02_PD4_GP74	BOARDID1	3VSB(+3V3_DSW_SIO)	H
115	SO3_PD5_GP75	2546_ILUM_R	3VSB(+3V3_DSW_SIO)	H
116	KS04_PD6_GP76	USB_PO_EN	3VSB(+3V3_DSW_SIO)	H
117	KS05_PD7_GP77	THERMTRIP_L_SIO	3VSB(+3V3_DSW_SIO)	H
118	SMBCLK4	NC		H
119	SMBDAT4	NC		H
120	FAN_CTL4_GP67	COM_AB_DET_N	3VSB(+3V3_DSW_SIO)	H
121	RTS1_GPOB0	RTS1_N	VCC3(+3V3_S0)	H
122	DSR1_GP81	DSR1_N	VCC3(+3V3_S0)	H
123	SOUT1_D_TX1_JP3	SOUT1_N	VCC3(+3V3_S0)	H
124	SIN1_D_RX1_GP83	SIN1_N	VCC3(+3V3_S0)	H
125	DTR1_GPOB4	DTR1_N	VCC3(+3V3_S0)	H
126	DCD1_GP85	DCD1_N	VCC3(+3V3_S0)	H
127	RI1_GP86	WOR_N	3VSB(+3V3_DSW_SIO)	H
128	CTS1_GP87	CTS1_N	VCC3(+3V3_S0)	H

PIN No.	AM4 Pin Name	Tiny 6 AMD Usage	Power Domain	Default H/L
AN5	PWR_BTN_L/AGPIO0	PWRBTN_OUT_SIO_N	VDD_33_S5(+3V3_S5)	H
AM4	SYS_RESET_L/AGPIO1	SYS_RESET_L	VDD_33_S5(+3V3_S5)	H
AL5	WAKE_L/AGPIO2	PCIE_WAKE_N	VDD_33_S5(+3V3_S5)	H
AT6	AGPIO3	WLAN_PCIE_WAKE_N	VDD_33_S5(+3V3_S5)	H
AR6	AGPIO4	APU_DELAYPCIERST_N	VDD_33_S5(+3V3_S5)	L
AP22	AGPIO5/DEVSLP0	SSD_PCIE_WAKE_N	VDD_33(+3V3_S0)	L
AN8	AGPIO6	M2_WLAN_DISABLE_N	VDD_33_S5(+3V3_S5)	L
AP7	AGPIO8	M2_BT_DISABLE_N	VDD_33_S5(+3V3_S5)	L
AN2	AGPIO9/SGPIO0_DATAOUT	LAN_PCIE_WAKE_N	VDD_33_S5(+3V3_S5)	L
AR3	SOA3_GPIO/AGPIO10/SGPIO0_CLK	+5V_S5_EN	VDD_33_S5(+3V3_S5)	H
AV13	BLINK/AGPIO11	PWR_LED_N	VDD_33_S5(+3V3_S5)	H
AL1	USB_OC0_L/AGPIO16	USB3_OC_N_0	VDD_33_S5(+3V3_S5)	H
AM1	USB_OC1_L/TDI/AGPIO17	USB3_OC_N_1	VDD_33_S5(+3V3_S5)	H
AR1	USB_OC2_L/TCK/AGPIO18	USB3_OC_N_2	VDD_33_S5(+3V3_S5)	H
AK3	SCL0/I2C3_SCL/AGPIO19	SMB_CLK_SECOND	VDD_33_S5(+3V3_S5)	OD
AK2	SDA1/I2C3_SDA/AGPIO20	SMB_DATA_SECOND	VDD_33_S5(+3V3_S5)	OD
AN3	AGPIO23/SGPIO_LOAD	DP_D_DET_N_R	VDD_33_S5(+3V3_S5)	H
AP1	USB_OC3_L/TDO/AGPIO24	SIO_SCI	VDD_33_S5(+3V3_S5)	H
AR4	AGPIO40/SGPIO0_DATAIN	SW_CLR_CMOS_N	VDD_33_S5(+3V3_S5)	H
AU17	SPI_TPM_CS_L/AGPIO76	SPI_TPM_CS_L	VDD_33(+3V3_S0)	H
AW21	SERIRQ/AGPIO87	LPC_SERIRQ	VDD_33(+3V3_S0)	H
AV22	GENINT1_L/AGPIO89	GENINT1_L_AGPIO89	VDD_33(+3V3_S0)	H
AU23	GENINT2_L/AGPIO90	TPM_SPI_IRQ_N_R	VDD_33(+3V3_S0)	H
AW23	SPKR/AGPIO91	APU_SPKR	VDD_33(+3V3_S0)	L
AT23	CLK_REQ0_L_SATA_ISO_L_SATA_ZP0_L_AGPIO92	PCIE_LAN_CLKREQ2	VDD_33(+3V3_S0)	H
AV24	CLK_REQ1_L/AGPIO115	PCIE_WLAN_CLK_REQ_N	VDD_33(+3V3_S0)	H
AT24	CLK_REQ2_L/AGPIO116	PCIE_SSD_CLK_REQ_N	VDD_33(+3V3_S0)	H
AM22	SATA_ACT_L/AGPIO130	SATA_LED_N	VDD_33(+3V3_S0)	H
AL7	PCIE_RST_L/EGPIO26	PCIE_RST_L_EGPIO26	VDD_33_S5(+3V3_S5)	H
AT18	EGPIO70	WWAN_POWER_OFF_N	VDD_33(+3V3_S0)	H
AU20	LPCLCK0/EGPIO74	CLK_SIO_33M	VDD_33(+3V3_S0)	L
AU19	LPCLCK1/EGPIO75	LPCLCK1	VDD_33(+3V3_S0)	H
AW11	EGPIO95	LAN_DISABLE_N	VDD_33(+3V3_S0)	L
AW12	EGPIO96	SSD_AUX_RST_N	VDD_33(+3V3_S0)	L
AW12	EGPIO97	DP1_DP_HDMI_N	VDD_33(+3V3_S0)	H
AU13	EGPIO98	DP2_DP_HDMI_N	VDD_33(+3V3_S0)	L
AV13	EGPIO99	DPD_DP_HDMI_N	VDD_33(+3V3_S0)	H
AT14	EGPIO100	LAN_AUX_RST_N	VDD_33(+3V3_S0)	L
AW20	LAD0/EGPIO104	LPC_AD0	VDD_33(+3V3_S0)	H
AV21	LAD1/EGPIO105	LPC_AD1	VDD_33(+3V3_S0)	H
AT21	LAD2/EGPIO106	LPC_AD2	VDD_33(+3V3_S0)	H
AT20	LAD3/EGPIO107	LPC_AD3	VDD_33(+3V3_S0)	H
AT15	ESPI_ALERT_L/LDRQ0_L/EGPIO108	LPC_DRQ0_N	VDD_33(+3V3_S0)	L
AW18	LFRAME_L/EGPIO109	LPC_FRAME_N	VDD_33(+3V3_S0)	H
AU25	SCL0/I2C2_SCL/EGPIO113	SMB_CLK_MAIN	VDD_33(+3V3_S0)	OD
AV25	SDA0/I2C2_SDA/EGPIO114	SMB_DATA_MAIN	VDD_33(+3V3_S0)	OD
AT17	SPI_CS1_L/EGPIO118	SPI_CS1_OUT_N_APU	+1V8_S5	H
AW15	SPI_CS2_L/ESPI_CS_L/EGPIO119	SPI_CS2_OUT_N	+1V8_S5	H
AV16	SPI_WP_L/ESPI_DAT2/EGPIO122	SPI_WP_N_APU	+1V8_S5	H
AL23	CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131	PCIE_SLOT_CLKREQ3	VDD_33(+3V3_S0)	H
AV15	SPI_HOLD_L/ESPI_DAT3/EGPIO133	SPI_HOLD_N_APU	+1V8_S5	H


SMB MAP




CLOCK DIAGRAM



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SIZE : A3	Date: Tuesday, April 28, 2020	PAGE: 65 of 66

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